Vertical GaN Power Devices: Device Principles and Fabrication Technologies—Part II

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***Abstract*— Vertical gallium nitride (GaN) power devices are enabling next-generation power electronic devices and systems with higher energy efficiency, higher power density, faster switching, and smaller form factor. In Part I of this review, we have reviewed the basic design principles and physics of building blocks of vertical GaN power devices, i.e., Schottky barrier diodes and p-n diodes. Key topics such as materials engineering, device engineering, avalanche breakdown, and leakage mechanisms are discussed. In Part II of this review, several more advanced power rectifiers are discussed, including junction barrier Schottky (JBS) rectifiers, merged p-n/Schottky (MPS) rectifiers, and trench metal–insulator–semiconductor barrier Schottky (TMBS) rectifiers. Normally-OFF GaN power transistors have been realized in various advanced device structures, including current aperture vertical electron transistors (CAVETs), junction field-effect transistors (JFETs), metal–oxide–semiconductor field-effect transistors (MOSFETs), and fin field-effect transistors (FinFETs). A detailed analysis on their performance metrics is provided, with special emphasis on the impacts of key fabrication processes such as etching, ion implantation, and surface treatment. Lastly, exciting progress has been made on selective area doping and regrowth, a critical process for the fabrication of vertical GaN power devices. Various materials characterization techniques and surface treatments have proven to be beneficial in aiding this rapid development. This timely and comprehensive review summarizes the current progress, understanding, and challenges in vertical GaN power devices, which can serve as not only a gateway for those interested in the field but also a critical reference for researchers in the wide bandgap semiconductor and power electronics community.**

***Index Terms*— Gallium nitride (GaN), junction barrier Schottky (JBS), power electronics, power transistors, selective area doping, wide bandgap (WBG) semiconductors.**

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I. Introduction

WIDE bandgap (WBG) semiconductor gallium nitride (GaN) has garnered considerable research interests for high-voltage, high-power, and high frequency applications [1]–[15], due to its large bandgap (3.4 eV), high critical electric field (3–4 MV/cm), high electron saturation velocity, and high Baliga's figure of merit. Fig. 1 shows a comparison of the ON-resistance and breakdown voltage for different semiconductors, including Si, GaAs, and the WBG semiconductor family. To realize the full potential of the GaN material in power electronics, the community has been transitioning from the lateral device geometry to a vertical one. The representative lateral device is the GaN high electron mobility transistors (HEMTs) grown on foreign substrates, which have reached a certain level of maturity and commercialization in the middle and low voltage applications. However, these lateral devices still suffer from surface-related current dispersion, poor heat dissipation, high defect densities, and inability to support avalanche breakdown [2], [3]. Due to the availability of bulk GaN substrates, vertical GaN power devices have been demonstrated with promising performance, such as high currents, high voltages, low defect densities, good thermal management, small chip area, and avalanche breakdown [12]–[18]. A typical vertical GaN power device is composed of a channel/contact layer, a drift layer, a buffer layer, and edge termination.

This review consists of two parts, presenting a comprehensive discussion on the recent development and current understanding and challenges of vertical GaN power devices. Their key device concepts, operation principles, crucial materials processes, fabrication technologies will be examined in detail. In Part I of this review, building blocks of vertical GaN power devices were studied, including GaN Schottky barrier diodes (SBDs) and p-n diodes. Materials engineering methods, device engineering approaches, avalanche breakdown, and leakage mechanisms in vertical GaN power devices were elucidated and analyzed. In Part II of this review, we discuss the development of more advanced vertical GaN power rectifiers, including junction barrier Schottky (JBS) rectifiers, merged p-n/Schottky (MPS) rectifiers, and trench metal–insulator–semiconductor barrier Schottky (TMBS) rectifiers.

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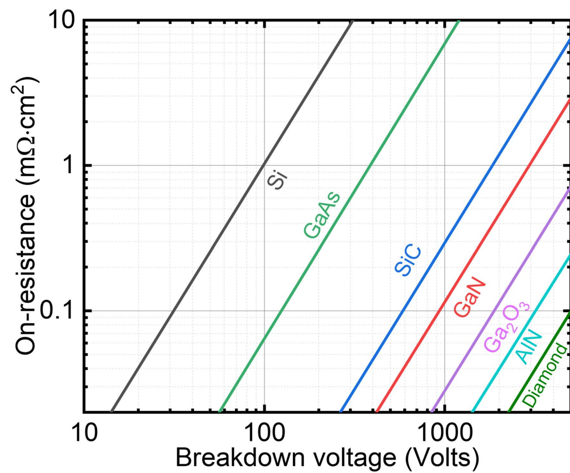

Fig. 1. ON-resistance versus breakdown voltage for Si, GaAs, and the WBG semiconductor family.

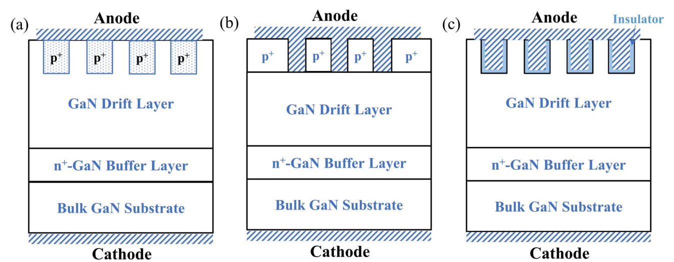

Fig. 2. Device schematics of (a) vertical GaN JBS or MPS rectifiers fabricated by ion implantation or regrowth, (b) trench vertical GaN MPS rectifiers fabricated via etching and without ion implantation, and (c) vertical GaN TMBS rectifiers.

Several important normally-OFF vertical GaN power transistors are also presented, including current aperture vertical electron transistors (CAVETs), junction field-effect transistors (JFETs), metal–oxide–semiconductor field-effect transistors (MOSFETs), and fin field-effect transistors (FinFETs). We also provide a detailed analysis on their device principles and performance metrics, highlighting the impacts of etching, ion implantation, and surface treatment. Lastly, we introduce the selective area doping and regrowth process, which is one of the most critical fabrication processes for vertical GaN power devices. This review can offer a systematic understanding of the state-of-the-art vertical GaN power devices and provide valuable insights for the future development of next-generation efficient, lightweight, and resilient power electronics.

II. Advanced Vertical GaN Power Rectifiers

Several advanced vertical GaN power rectifiers were developed to overcome the limitations of basic GaN SBDs and p-n diodes and to offer better device performance. The limitations of basic SBDs include large reverse leakage and low breakdown voltage, while the drawbacks of basic p-n diodes are high forward voltage drop and large reverse recovery current. Advanced vertical GaN rectifiers are expected to address these shortcomings and offer a better balance in performance tradeoffs between forward voltage drop, reverse recovery current, leakage current, and breakdown voltage [19]. To date, advanced devices such as vertical GaN JBS rectifiers [Fig. 2(a)], vertical GaN MPS rectifiers [Fig. 2(a) and (b)], vertical trench metal–insulator–semiconductor (MIS), and barrier Schottky (TMBS) rectifiers [Fig. 2(c)] have been demonstrated.

The device schematic for vertical GaN JBS rectifiers is shown in Fig. 2(a), which features an array of alternating p-GaN and n-GaN regions at the top portion of the GaN JBS rectifiers. In order to simplify the fabrication processes, the same anode Schottky metals were usually used to form contacts to both the p-GaN and n-GaN regions without any annealing process. JBS rectifier is a unipolar device that has a turn-on voltage similar to that of an SBD. This is because the p-n junction is not turned on during forward bias. The distance between the p-type regions must be properly designed to *not* fully deplete the n-GaN region during forward bias to achieve unipolar conduction [19]. Compared with the basic SBDs, JBS rectifiers have reduced reverse leakage current and enhanced breakdown voltage. This is because the Schottky contact in the JBS devices is shielded from the high electric field due to the potential barrier created by the p-n junction around the Schottky contact. And a smaller electric field at the Schottky contact will result in a smaller Schottky barrier lowering and a weaker field emission effect, leading to low leakage current and high breakdown voltage.

Vertical GaN JBS rectifiers were first demonstrated by Zhang *et al.* [20] using ion implantation via two methods. The first method was implanting Mg into n^--GaN or i-GaN of i-n structure to form p-wells [Fig. 3(a)], and the other one was implanting Si into p-GaN of the p-i-n structure to form n-wells [Fig. 3(b)]. The cross-sectional scanning electron microscopy (SEM) images confirmed the formation of p-wells [Fig. 3(c)] and n-wells [Fig. 3(d)] in these devices. Both Mg-implanted and Si-implanted JBS rectifiers had low turn-on voltages (<1 V) that were similar to that of the SBDs. The ON-resistance of the JBS rectifiers was higher than that of the basic vertical GaN SBDs [Fig. 3(e) and (f)]. This was due to the use of the n-GaN area for forward conduction and nonuniform current distributions, leading to larger channel resistance and spreading resistance, respectively. The breakdown voltage of the JBS rectifiers was larger than that of the SBDs, but smaller than that of the p-n diodes [Fig. 3(g) and (h)]. In addition, the device performance metrics of the JBS devices could be further tuned by modifying the width of n- or p-wells. Increasing n-well width and decreasing p-well width could reduce ON-resistance, forward voltage, and breakdown voltage of the JBS devices.

Vertical GaN MPS rectifiers have similar structures as the vertical JBS rectifiers except that the ohmic contacts are formed between the anode metals and the p-GaN regions in the MPS devices. Compared with basic vertical p-n diodes, MPS rectifiers show smaller forward voltage drop, smaller reverse recovery current, and less power switching loss [19]. Compared with JBS devices, MPS rectifiers show better surge current capability [21]. However, MPS rectifiers have larger

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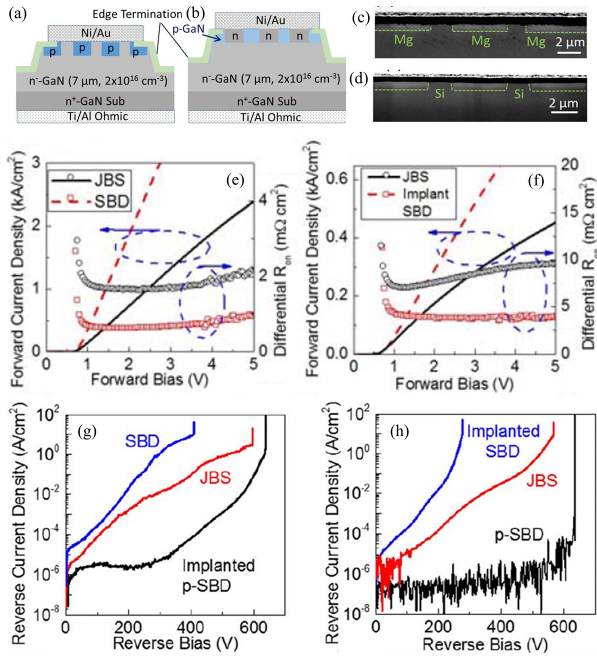

Fig. 3. Schematics of (a) Mg-implanted GaN JBS rectifiers and (b) Si-implanted GaN JBS rectifiers. SEM images of the cross section of (c) Mg-implanted and (d) Si-implanted GaN JBS rectifiers. Forward $I-V$ characteristics and ON-resistance of (e) Mg-implanted JBS rectifiers and conventional SBDs and (f) Si-implanted JBS rectifiers and SBDs. Reverse $I-V$ characteristics of JBS rectifiers, conventional SBDs, and implanted SBDs in (g) Mg-implanted samples and (h) Si-implanted samples. Reprinted from [20] with permission, [2017] IEEE.

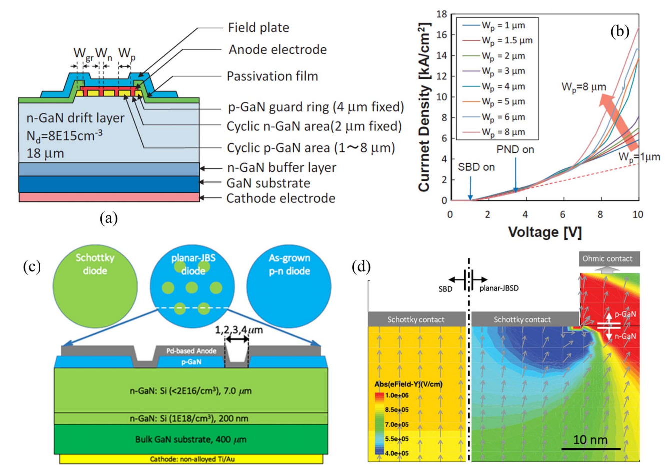

Fig. 4. (a) Cross-sectional device structure of trench GaN MPS rectifiers via partial p-GaN removal in a standard GaN p-i-n diode structure. (b) Forward $I-V$ characteristics of trench GaN MPS rectifiers with different p-GaN region widths. (c) Top view and cross section of trench MPS rectifiers with circular trenches for Schottky contacts. (d) Simulated electric field distributions of conventional SBDs (left) and trench MPS rectifiers (right) at −200 V. (a) and (b): Reprinted from [21] with permission. Copyright (2017) The Japan Society of Applied Physics. All rights reserved. (c) and (d): Reprinted from [22] with permission, [2017] IEEE.

reverse recovery current than JBS devices due to minority carrier injection through the ohmic contacts, which leads to slower frequency responses in the devices.

Hayashida *et al.* [21] reported a vertical trench GaN MPS rectifier using etching processes instead of ion implantation. The fabrication process involved selectively etching away part of the p-GaN from the basic vertical p-n diodes to expose the underlying n-GaN [Fig. 4(a)], where the anode metal contacts were deposited. The device had a patterned surface with concentric patterns, although a planar device is more preferred for power electronics. Under forward bias [Fig. 4(b)], the Schottky junction was first turned on at low voltages, and then the p-n junction was turned on at high voltages. With increasing p-GaN region width [Fig. 4(b)], the ON-current of the device increased due to stronger minority carrier injection. When the p-GaN region width was increased, the breakdown voltage of the device also increased, while the reverse leakage current of the device decreased. The vertical GaN MPS rectifiers with a drift layer thickness of 18 μm showed a breakdown voltage of 2 kV and an ON-resistance of 1.7 m$\Omega\cdot$cm^2. Furthermore, Li *et al.* [22] also proposed a similar vertical GaN MPS rectifier with circular trenches for Schottky contacts [Fig. 4(c)]. The device showed much-reduced leakage current, which was ascribed to the reduced surface field (RESURF) effect. This is because the p-GaN at the edge of the trenches extended its depletion region under the Schottky contacts, reducing the electric field under the Schottky contacts [Fig. 4(d)].

Vertical GaN TMBS rectifiers are another type of unipolar vertical GaN power devices, which were first reported by Zhang *et al.* [23], [24]. Similar to JBS devices, TMBS rectifiers use MIS structures (usually in trenches that are adjacent to Schottky contacts) to generate potential barriers via their depletion regions to shield Schottky contracts from high electric fields [19]. Compared with basic SBDs, TMBS rectifies exhibited larger breakdown voltage and smaller reverse leakage current. Zhang *et al.* [23] added additional field rings [Fig. 5(a)] in the trenches to improve the breakdown voltage and reverse leakage [Fig. 5(b)]. The geometries of the trench structures are key design parameters for GaN TMBS rectifiers, including mesa widths and trench shapes. Devices with smaller mesa width (i.e., closer trenches) exhibited larger breakdown voltage and smaller reverse leakage current. This is due to stronger MIS depletion effects in the mesa as verified by electric field distributions in the devices [23]. In terms of trench shapes, it was found that varying dry etching conditions combined with tetramethylammonium hydroxide (TMAH) wet etching could result in different trench shapes [Fig. 5(c)]. A comparison between the device's performance of different vertical GaN TMBS rectifiers with flat-bottom rounded trenches, tapered-bottom rounded trenches, and nonrounded trenches showed that GaN TMBS rectifiers with flat-bottom rounded trenches showed the lowest leakage current and the highest breakdown voltage. This is because this trench shape has the most uniform distribution of electric field and the lowest peak electric field, as shown in simulation results in Fig. 5(d)–(f). With 7 μm drift layer, the vertical GaN TMBS rectifiers showed a turn-on voltage of 0.8 V, an ON-resistance of 2 m$\Omega\cdot$cm^2, and a breakdown voltage of ∼700 V.

Fig. 6 shows the benchmark plot for reported vertical GaN JBS, MPS, and TMBS rectifiers on bulk GaN substrates [20].

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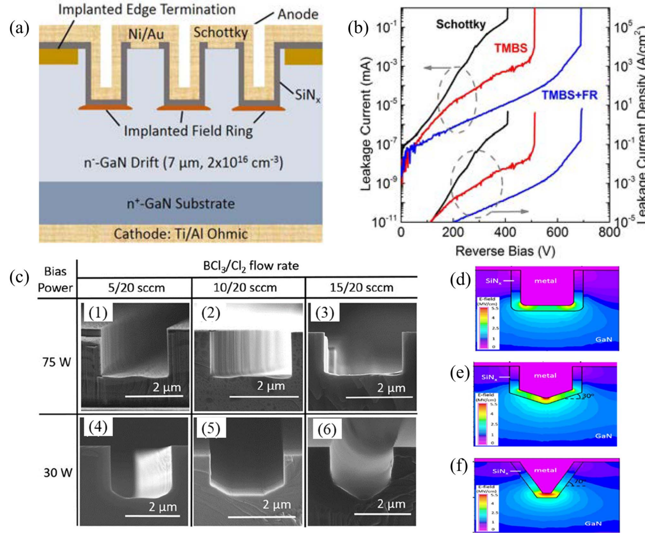

Fig. 5. (a) Schematic of vertical GaN TMBS rectifiers with implanted field rings (FRs) in the trenches. (b) Leakage current and leakage current density of TMBS rectifiers, TMBS rectifiers with FR, and conventional SBDs. (c) Cross-sectional SEM images of trench shapes using different dry etching conditions. (d)–(f) Simulated electric field distributions in nonrounded trench, rounded flat-bottom trench, and rounded tapered-bottom trench at −600 V, respectively. (a) and (b): Reprinted from [23] with permission, [2017] IEEE. (c)–(f): Reprinted from [24] with the permission of the American Institute of Physics (AIP) Publishing.

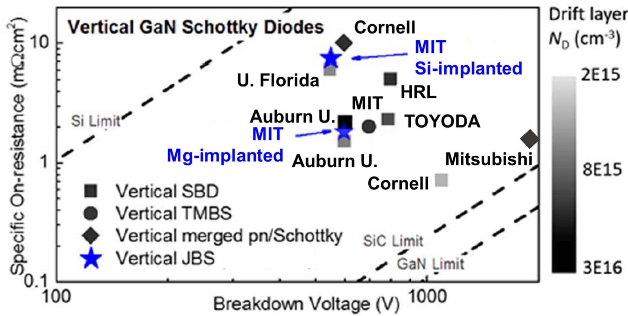

Fig. 6. ON-resistance versus breakdown voltage for reported advanced vertical GaN power rectifiers and conventional SBDs. Reprinted from [20] with permission, [2017] IEEE.

III. NORMALLY-OFF VERTICAL GaN POWER TRANSISTORS

Various vertical GaN power transistors have been developed to realize normally-OFF devices due to their failure-safe operation and simple driving circuits in power electronics applications, including CAVETs (e.g., p-GaN-gated CAVETs and trench CAVETs) [Fig. 7(a)–(c)], trench MOSFETs [Fig. 7(d) and (e)], and FinFETs [Fig. 7(f)], and JFETs.

Vertical GaN CAVETs were developed based on AlGaN/GaN heterostructures with the addition of buried current blocking layers (CBLs) in the drift layer to form a current aperture. Polarizations from this heterostructure create a lateral two-dimensional electron gas (2DEG) channel in the source access region. When the bottom drain is positively biased, electrons from the source move laterally through the 2DEG channel and then vertically through the aperture

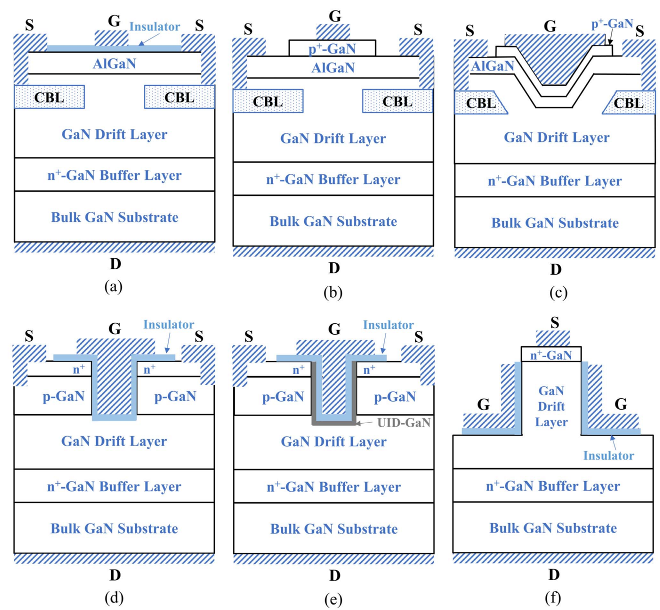

Fig. 7. Schematics of three versions of vertical GaN CAVETs: (a) conventional CAVETs; (b) p-GaN-gated CAVETs; and (c) trench CAVETs with p-GaN gate. The device schematics of (d) vertical GaN trench MOSFETs, (e) OG-FETs, and (f) FinFETs. S, D, G denote source, drain, and gate, respectively.

formed by the CBLs [2], [25]. The first normally-OFF GaN CAVET with a threshold voltage of 0.6 V was demonstrated by Chowdhury *et al.* [26] on sapphire substrates using Mg-implanted p-GaN as the CBLs. CF_4 plasma treatment was applied to the devices to help deplete the 2DEG channel and achieve normally-OFF operation. Furthermore, due to the Mg out-diffusion issue in the implanted p-GaN during high-temperature metalorganic chemical vapor deposition (MOCVD) regrowth, epitaxially grown p-GaN was used as CBLs in GaN CAVETs. Nie *et al.* [27] demonstrated p-GaN-gated GaN CAVETs [Fig. 7(b)] with *in situ* grown p-GaN by MOCVD as the CBLs, where the p-GaN gate was used to increase the threshold voltage. During device operation, the buried p-GaN CBLs were connected to the source to keep it at zero potential and avoid floating body effects. The device showed a breakdown voltage of 1.5 kV, an ON-resistance 2.2 m$\Omega \cdot$cm^2, and a threshold voltage of 0.5 V.

However, these CAVET devices were fabricated on polar *c*-plane planar channels with high electron concentrations in the 2DEG channels, which led to low threshold voltages (e.g., <1 V) in the devices. To circumvent this issue, p-GaN-gated GaN trench CAVETs with a slanted semipolar plane channel [Fig. 8(a) and (b)] was developed by Shibata *et al.* [28]. Fig. 8(c) shows a comparison of the band diagrams of the devices with a slanted semipolar plane channel and those with a polar (0001) *c*-plane channel. The Fermi level in the slanted channel devices was moved up, which means that there were few free electrons in the slanted channel. Compared with the polar *c*-plane, the polarization-induced charges on the semipolar planes are much reduced [29]–[32], resulting in a lower concentration of 2DEG in the semipolar channel. The 2DEG concentration in the slanted channel decreased, and the threshold voltage increased with increasing

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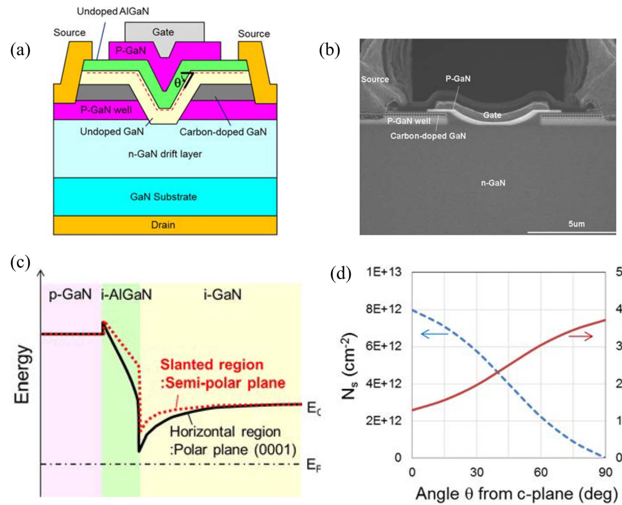

Fig. 8. (a) Schematic and (b) cross-sectional SEM image of the device of GaN CAVETs with MOCVD-regrown semipolar channels. (c) Band diagrams of the CAVETs with a semipolar slanted channel and a polar c-plane channel at zero gate bias. (d) Simulated 2DEG concentration (N_S) and threshold voltage as a function of channel plane inclination angle θ from the c-plane. Reprinted from [28] with permission, [2016] IEEE.

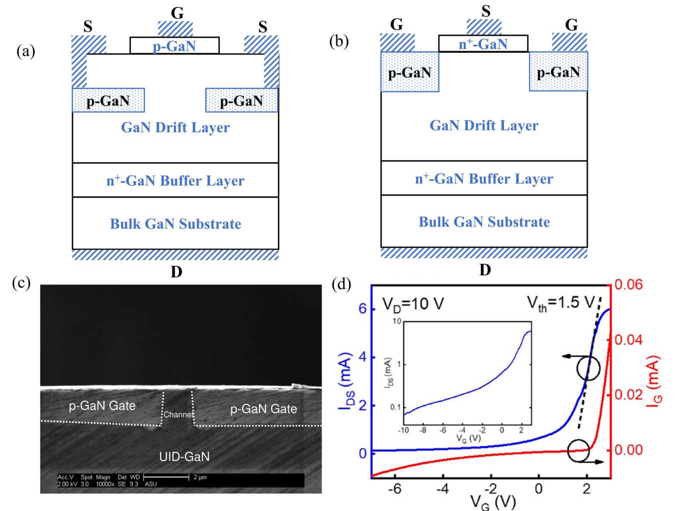

Fig. 9. Device schematics of (a) lateral channel GaN JFETs and (b) vertical channel GaN JFETs. (c) Cross-sectional SEM image of the fabricated vertical channel GaN JFETs. (d) Transfer characteristics and gate leakage of the demonstrated vertical channel GaN JFETs. (c) and (d): Reprinted from [36] with permission, [2020] IEEE.

plane inclination angle θ away for the c-plane [Fig. 8(d)]. This trend is caused by the decreasing polarization changes in GaN planes with increasing plane inclination angle [29]–[32]. As a result, a threshold voltage of over 2 V was realized in these slanted channel devices compared with that of 1 V in those without slanted channels. Furthermore, the carbon-doped GaN layer above the p-GaN well was also effective in suppressing punchthrough current and increasing breakdown voltage. With a 13-μm drift layer, the vertical trench CAVETs had a breakdown voltage of 1.7 kV, and an ON-resistance of 1.0 m$\Omega\cdot$cm^2, and a threshold voltage of 2.5 V. Moreover, normally-OFF MIS gate GaN trench CAVETs were also reported [33].

JFETs use p-n junctions as the gate to deplete the channel and realize normally-OFF operation [Fig. 9(a) and (b)] without the need for gate dielectrics. However, compared to the mature technology of Si and SiC JFETs, GaN JFETs are still in their inception. The gate voltage of JFETs is usually limited to the bandgap voltage of the semiconductor to prevent the turn-on of the gate p-n junction. Due to GaN's large bandgap, GaN JFETs will have a larger gate voltage window. Ji and Chowdhury [34] carried out a comprehensive study on the design of lateral channel JFETs [Fig. 9(a)] and vertical channel JFETs [Fig. 9(b)] using device TCAD simulation. Kizilyalli and Aktas [35] experimentally demonstrated normally-ON GaN lateral channel JFETs. Recently, Yang *et al.* [36] reported normally-OFF GaN vertical channel JFETs with MOCVD regrown p-GaN gate [Fig. 9(c)], where the devices showed a threshold voltage of 1.5 V [Fig. 9(d)]. And the device performance could be impacted by the crystal orientation of the channel. The devices also showed some performance degradation caused by the nonideal effects in the MOCVD regrowth, such as interfacial impurities and nonuniform acceptor distribution in the regrown p-GaN gate. In addition, Kotzea *et al.* [37] demonstrated a quasi-vertical GaN JFET on sapphire substrates. However, the devices were normally-ON and had low ON–OFF ratio. Due to challenges in MOCVD regrowth, GaN JFETs still suffer from large device leakage and low breakdown voltage, where significant research efforts are still required.

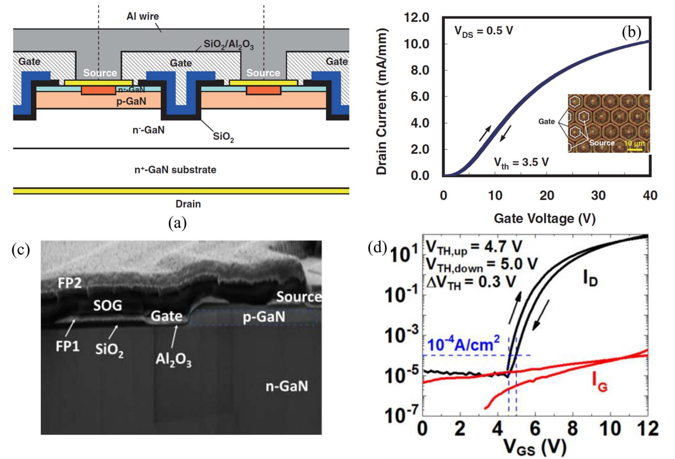

Fig. 10. (a) Schematic cross section of the GaN trench MOSFETs. (b) Transfer characteristics of the GaN trench MOSFETs. The inset shows the top view of the fabricated GaN trench MOSFETs with a hexagonal gate layout. (c) Cross-sectional SEM image of GaN OG-FETs with double field plates. (d) Transfer characteristics and gate leakage of the GaN OG-FETs. (a) and (b): Reprinted from [39] with permission. Copyright (2015) The Japan Society of Applied Physics. All rights reserved. (c) and (d): Reprinted from [42] with permission, [2017] IEEE.

Vertical GaN trench MOSFETs have two back-to-back p-n junctions from the source to the drain; therefore, no current flows without gate bias, i.e., they are normally-OFF devices. The buried p-GaN body in the devices is also shorted to the source contact to prevent floating body effects. Otherwise, a high drain bias can lead to a nonzero positive potential in the p-GaN, leading to reduced threshold voltage and increased

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leakage current. Oka *et al.* [38], [39] demonstrated the first GaN trench MOSFETs [Fig. 10(a)] with a high threshold voltage (>5 V), a breakdown voltage of 1.6 kV, and an ON-resistance of 12.1 mΩ·cm^2. Furthermore, they used a hexagonal trench gate layout [Fig. 10(b)] to increase the gate width per unit area, which increased the drain current, reduced the ON-resistance, and decreased the threshold voltage in the devices. This design resulted in a GaN trench MOSFET with a threshold voltage of 3.5 V, an ON-resistance of 1.8 mΩ·cm^2, and a breakdown voltage of 1.2 kV. It should be noted that the interfacial charges between the gate dielectric and the trench play a critical role in determining the threshold voltage of the devices. These charges may come from nitrogen vacancies due to the trench etching process and residual impurities such as O and Si [40], [41].

Despite these encouraging results, GaN trench MOSFETs face two challenges in fabrication and device operation: 1) the channel mobility along the p-GaN inversion layer is very low due to the interface and impurity scattering. As a result, an abnormally large gate bias (e.g., >30 V) is required to gain a reasonable drain current in the devices. 2) It is very difficult to form good ohmic contacts in the buried p-GaN body after the plasma etching process due to the generation of n-type compensating vacancies. To circumvent the first challenge, *in situ* oxide GaN interlayer vertical trench MOSFETs (OG-FETs) were demonstrated [42], [43], where a thin unintentionally doped (UID) GaN (UID-GaN) interlayer was grown in the trench as the channel [Fig. 10(c)]. This channel had much higher electron mobility due to suppressed interface scattering with the oxide layer, and reduced impurity scattering due to the low doping concentration in the UID GaN channel. High-performance vertical trench MOSFETs are, therefore, possible with these new fabrication processes. GaN OG-FETs with a threshold voltage of 4.7 V [Fig. 10(d)], an ON-resistance of 2.2 mΩ·cm^2, and a breakdown voltage of 1.4 kV were demonstrated [42]. To solve the second challenge, Li *et al.* [44] replaced the etching process (which was used for accessing the buried p-GaN) with selective area regrowth on the n$^+$-GaN source layer using MOCVD, where a via to the buried p-GaN was formed for body contacts.

Furthermore, Tanaka *et al.* [45] realized planar vertical GaN MOSFETs using all ion implantation processes. To obtain better implanted p-GaN, they applied Mg and N sequential implantation to form a p-type layer. Mg/N-implanted p-GaN exhibited similar Mg concentration profiles to Mg-implanted p-GaN before and after annealing. It was found that GaN p-n junction with Mg/N implanted p-GaN showed increased breakdown voltage and decreased leakage current, compared with p-n junction with only Mg-implanted p-GaN. This performance enhancement was likely because the N sequential implantation reduced the hole traps in the p-GaN due to N vacancies. Based on these results, they fabricated planar vertical GaN MOSFETs using Mg/N implantation for p-well, Si implantation for n-well, and O implantation for the JFET region to reduce the JFET resistance. The devices showed a threshold voltage of 2.5 V, an ON-resistance of 1.4 mΩ·cm^2 (2.8 mΩ·cm^2 if including the source parasitic resistance), and a breakdown voltage of 1.2 kV [45].

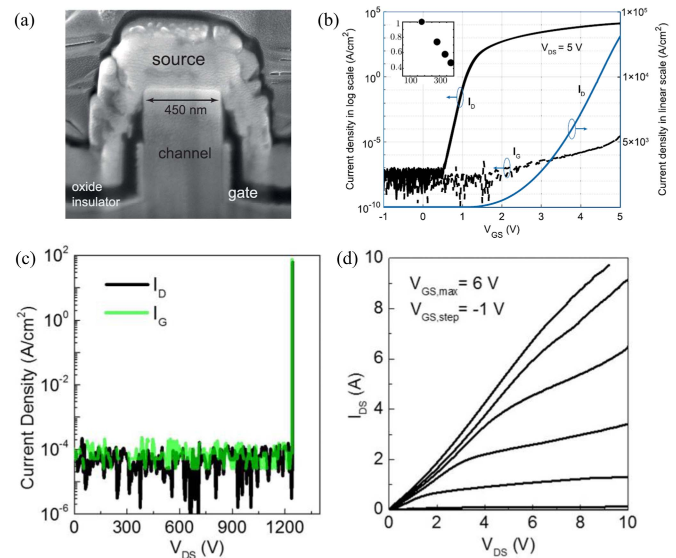

Fig. 11. (a) Cross-sectional SEM image of GaN FinFETs. (b) Transfer characteristics and gate leakage of GaN FinFETs with a fin width of 180 nm. (c) OFF-state drain and gate leakage of GaN FinFETs at zero gate bias. (d) Output characteristics of 10-A GaN FinFETs with >600 fins (fin width 250 nm). (a) and (b): Reprinted from [46] with permission, [2017] IEEE. (c) and (d): Reprinted from [47] with permission, [2017] IEEE.

Vertical GaN FinFETs can also offer normally-OFF operation [5] without the need for p-GaN. When the fin width is down to several hundred nanometers, the fin channel can be depleted by the work function difference between the gate metal and GaN [46]. The threshold voltage of the devices will increase with decreasing fin width due to stronger depletion effects. However, in the device fabrication, electron beam lithography has to be used to define the narrow fin patterns. Furthermore, dry etching and TMAH etching must be used together to achieve a vertical fin profile [46] for good gate modulation. The crystal orientation of the fin can also affect the sidewall roughness of the fins after etching. All these factors significantly increase the complexity and cost of FinFET fabrication. Despite these challenges, vertical GaN FinFETs have been developed [Fig. 11(a) and (b)]. Zhang *et al.* [47], [48] showed kV-class GaN FinFETs and large-area devices with a current of 10 A [Fig. 11(c) and (d)] and a high switching figure of merit. Furthermore, Xiao *et al.* [49] systematically investigated the leakage and breakdown mechanisms of vertical GaN FinFETs. A high potential barrier in the fin channel at high drain bias was found to be critical for normally-OFF device operation, since the potential barrier can be reduced by the drain-induced barrier lowering (DIBL) effect, which is closely related to fin geometry, fin/oxide interface charge, and gate–drain bias. In addition, the ON-resistance of the GaN FinFETs was also analyzed [50], where the dominant resistance stemmed from the drift layer and the substrate.

In a short summary, the four types of normally-OFF vertical GaN power transistors discussed in this section have their distinct advantages and disadvantages.

1) **GaN CAVETs:** Due to the 2DEG channel, GaN CAVETs exhibit high channel electron mobility and

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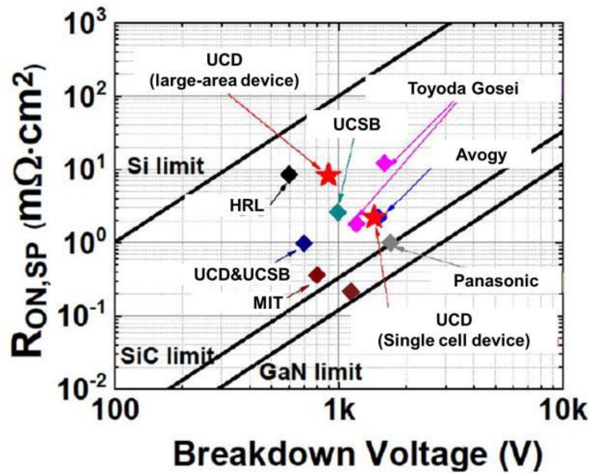

Fig. 12. ON-resistance versus breakdown voltages of vertical GaN power transistors. Reprinted from [42] with permission, [2017] IEEE.

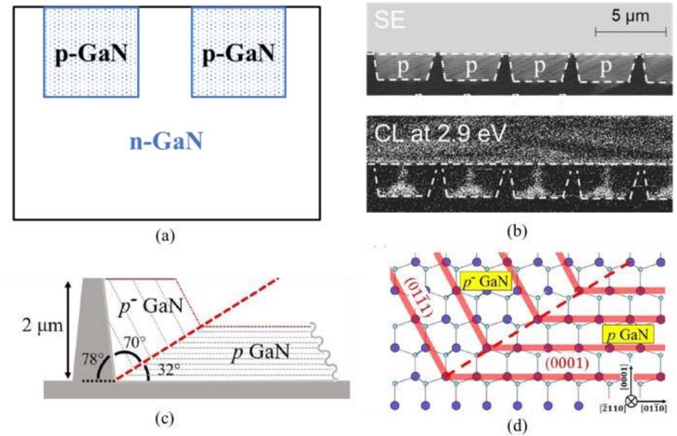

Fig. 13. (a) Schematic of the selective area doping and regrowth process and the resulted laterally patterned p-n junctions. (b) SE image and CL of p-GaN regrowth in trenches. Low CL intensity at 2.9 eV indicates low acceptor concentration. (c) Schematic of the p^--GaN lateral growth from the trench sidewall and the p-GaN vertical growth from the trench base. (d) Crystal planes of the two growth fronts and their boundary indicated by the dashed line. Reprinted from [58] with the permission of AIP Publishing.

high current. However, they have complicated device structures (e.g., p-GaN CBLs, regrown AlGaN/GaN channels, and slanted semipolar plane channels), which require significant efforts in epitaxial regrowth and are challenging to fabricate.

2) **GaN JFETs:** Normally-OFF operation can be achieved in JFETs without any gate dielectrics. However, their gate bias is limited to <3.5 V to prevent the turn-on of parasitic gate p-n junctions. In addition, the regrowth of the p-GaN gate is also very challenging.

3) **GaN trench MOSFETs:** These devices have very simple device structures that do not require regrowth, and high threshold voltages can be obtained. Their disadvantages include low channel mobility, interface charges at the trench sidewall (caused by dry etching and dielectrics deposition), high gate bias required to achieve decent drain currents, and the difficulty in forming good ohmic contacts in the buried p-GaN body after dry etching. The low mobility issue could be partially solved by the OG-FETs with the regrown UID-GaN channel.

4) **GaN FinFETs:** The advantage of GaN FinFETs is that they have no p-GaN layers in the devices and do not require the regrowth process. However, the device fabrication process involves the use of electron beam lithography, which is complicated and costly, with potentially low device throughput and low device yield.

Fig. 12 shows the benchmark plot and comparison of reported vertical GaN power transistors on bulk GaN substrates [42], [43], [47].

IV. Selective Area Doping and Regrowth

Selective area doping and regrowth is an essential material process for the fabrication of vertical GaN power rectifiers and transistors. Selective area doping is required to produce laterally pattern p-n junctions [Fig. 13(a)], which are the foundations fabricating junction termination extension (JTE), JBS, and MPS rectifiers, JFETs, U-shape MOSFETs (U-MOSFETs), and superjunctions. Historically, ion implantation was used to fabricate these structures for Si and SiC power devices, which has reached a high level of maturity. However, ion implantation is challenging for GaN due to the required high annealing temperatures (>1000 °C), which are beyond the GaN decomposition temperature (~900 °C). Recent efforts in suppressing GaN decomposition at high annealing temperatures include AlN capping layers, multicycle rapid thermal annealing [51], [52], ultrahigh pressure [53]–[55], and Mg and N sequential implantation [45], [56]. However, effective ion implantation, especially for p-type GaN [53]–[55], remains a challenge. As a result, the regrowth process via MOCVD or molecular beam epitaxy (MBE) on trench structures with smooth and low-defect sidewalls by proper etching [57] is widely regarded as one of the most promising methods to achieve selective area doping in GaN.

A typical selective area regrowth process includes the growth of n-GaN layers, trench formation in n-GaN by etching, and regrowth of p-GaN [Fig. 13(b)]. It was found that p-GaN regrowth in the trench [58] was composed of fast lateral growth from the trench sidewall and slow vertical growth from the trench base [Fig. 13(c) and (d)]. Material characterizations [58], [59] using secondary electron (SE) imaging and cathodoluminescence (CL) showed that the acceptor concentration in the regrown p-GaN was not uniformly distributed, with much lower acceptor concentration in the sidewall [Fig. 13(b)]. In addition to growth optimization, shallow trenches were found to be effective in suppressing the unwanted lateral growth and the nonuniform acceptor distribution, possibly due to the faster coalesce of the lateral and vertical growth fronts.

Currently, most regrown p-n junctions have shown large reverse leakage currents and low breakdown voltages, possibly due to dry etching damage and the resulting poor regrowth interface. Transmission electron microscope (TEM) images of the regrown p-n junctions showed the regrowth interface [Fig. 14(a)]. Secondary ion mass spectrometry (SIMS)

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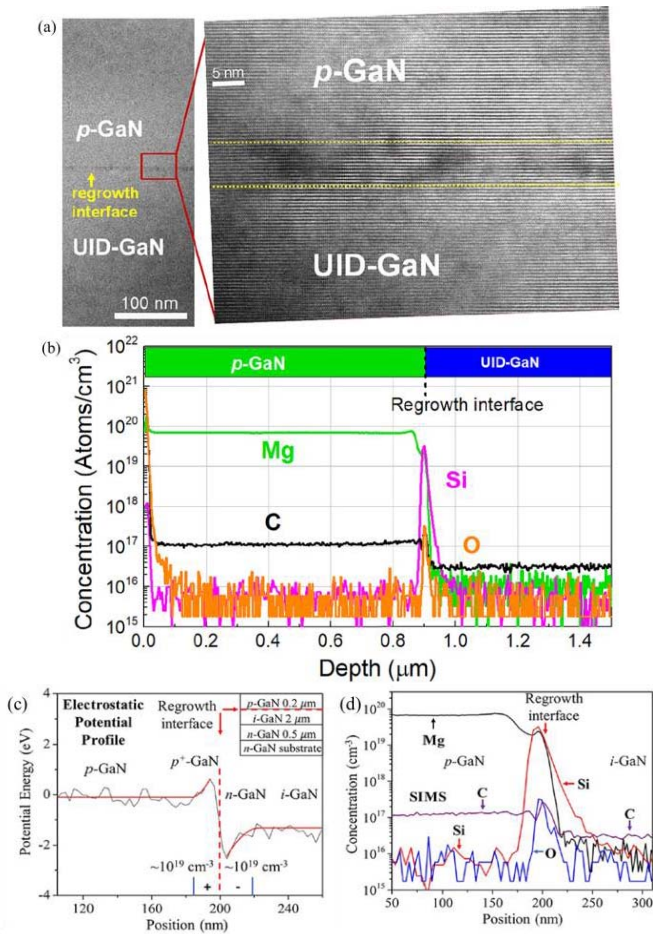

Fig. 14. (a) Cross-sectional TEM image and (b) SIMS profile of the regrown p-n junction. The regrowth interface is clearly visible. (c) Electrostatic potential profile near the regrowth interface in a regrown GaN p-i-n structure obtained by electron holography with charge densities near the regrowth interface indicated. (d) SIMS profile of the near the regrowth interface in (c). (a) and (b): Reprinted from [60] with the permission of AIP Publishing. (c) and (d): Reprinted from [61] with the permission of AIP Publishing.

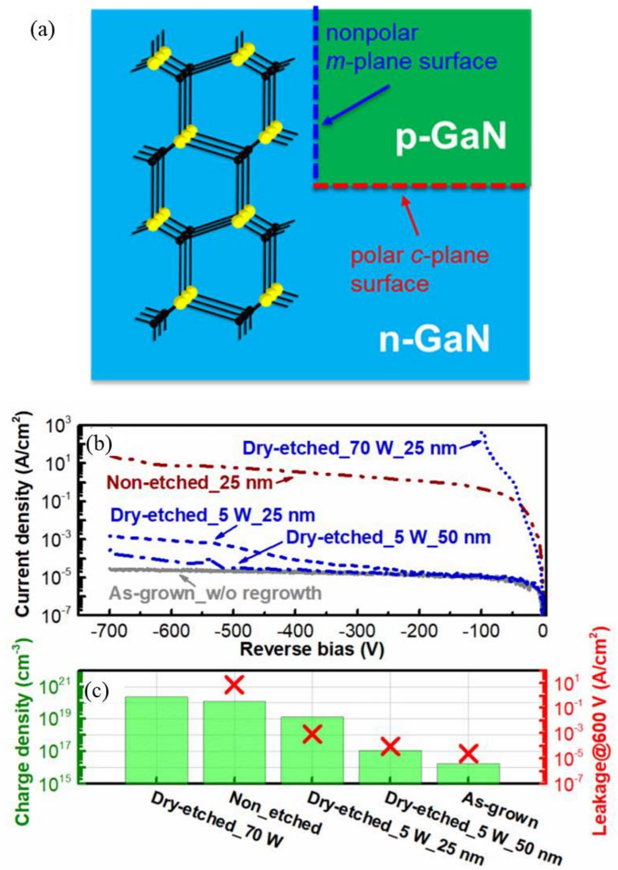

Fig. 15. (a) Schematic of regrown p-n junctions in a trench structure where the lateral and vertical junctions are from different crystal orientations. (b) Reverse $I-V$ regrown p-n junctions with different dry etching conditions and different insertion layer thickness. (c) Charge density at the regrowth interface and leakage current for the five regrown p-n junctions in (b). Reprinted from [65] with permission, [2019] IEEE.

analysis [Fig. 14(b)] confirmed that a large number of impurities, such as Si and O (sources for donors), were observed at the regrowth interface [60]. It should be noted that Mg concentration peak was also observed at the regrowth interface, indicating Mg gettering [61]. Capacitance–voltage $(C-V)$ measurements are commonly used to investigate the distribution of charges in devices [62], [63]. A high concentration of charges at the regrowth interface was observed using $C-V$ measurements [60]. The effect of these high-density charges on the band profile of the regrown p-n junctions was revealed by electron holography [Fig. 14(c)], where considerable band bending occurred at both sides of the regrowth interface [61]. The band bending at the n-side was due to Si and O impurities, while the band bending at the p-side was likely due to the high concentration of holes from Mg/Si [Fig. 14(d)] and Mg/O codoping [64]. These findings were used to explain the large leakage current in regrown GaN p-n junctions, i.e., the regrowth interface may act as a leaky $p^+/-n^+$ tunneling junction [61].

Due to the complexity of p-GaN regrowth in trench structures involving two crystal orientations [Fig. 15(a)], researchers tried to simplify the process by directly regrowing p-GaN on etched planar surfaces for regrown vertical p-n junctions, the properties of which can be used to study the regrowth process [60], [65]–[67]. A smooth and low-damage etching is the key process to achieve an excellent regrowth interface. Inductively coupled plasma (ICP) dry etching is one of the most widely used etching methods. Studies on the effects of ICP etching and surface treatment on the regrown p-n junctions were carried out [65], highlighting the following three key approaches:

First, proper surface treatment before the regrowth process is critical. Fu *et al.* [65] reported a surface treatment process for the regrown GaN p-n junctions using UV-ozone, and HF and HCl acid treatment. The UV-ozone will first oxidize the GaN surfaces and organic contaminants, and the acids will then help remove oxidized materials, which results in a clean regrowth surface. In addition, Pickrell *et al.* [68] also reported an effective surface treatment method using dilute KOH.

Second, reducing ICP etching power can dramatically reduce the interface charges, leading to much smaller leakage currents in the regrown p-n junctions [Fig. 15(b) and (c)]. Furthermore, an additional thermal annealing process can effectively remove residual etching reaction byproducts

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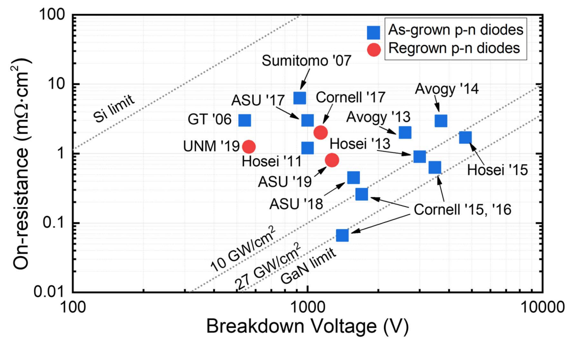

Fig. 16. Comparison of vertical GaN regrown and as-grown p-n diodes. Reprinted from [65] with permission, [2019] IEEE.

(e.g., $GaCl_x$), therefore reducing surface roughness and improving regrowth interfaces [69]. It is also worth noting that other innovative etching methods have also been developed to minimize the etching damage, including atomic layer etching (ALE) and *in situ* etching [70], [71].

Third, a thin UID-GaN insertion layer can be grown before the p-GaN regrowth, which can effectively decrease the leakage current in the regrown p-n junctions. This is because this UID-GaN insertion layer can shift the junction away from the regrowth interface, preventing the formation of leaky $p^+/-n^+$ tunneling junctions.

Using a combination of the abovementioned three approaches, the leakage current density in the regrown GaN p-n junctions to the order of 10^{-5} A/cm^2 [65], which is close to the value in as-grown p-n junctions (i.e., without the regrowth process). However, one drawback of this low power ICP etching is the low etching rate (i.e., 1 nm/min), which is not practical for structures with deep trenches and mesas. Therefore, a multistep etching process (i.e., steps with decreasing ICP etching powers) was developed to balance the etching rate and the etching damage. Regrown devices fabricated using this multistep etching process [65] showed excellent device performance with an on/off ratio of $\sim 10^{10}$ and a high breakdown voltage of >1.2 kV. Baliga's figure of merit of this device was 2.0 GW/cm^2, which is comparable to as-grown p-n diodes. In addition, Hu *et al.* [72] reported a regrown p-n diode with a breakdown voltage of 1.1 kV using MBE regrowth. Monavarian *et al.* [73] showed a regrown p-n diode on nonpolar m-plane substrates with a breakdown voltage of 540 V.

Fig. 16 shows a comparison of the performance of vertical GaN regrown p-n diodes with some as-grown p-n diodes on bulk substrates [65]. The performance of GaN regrown p-n junctions is expected to be further improved by optimizing etching conditions, surface treatments, and regrowth processes. And high quality lateral regrown p-n junctions can be developed by capitalizing on these results to realize selective area doping for advanced GaN power electronics.

V. Conclusion

This article reviews the recent development of vertical GaN power rectifiers and transistors, highlighting their unique device principles and advanced fabrication technologies. Various advanced vertical GaN power rectifiers are demonstrated, such as JBS, MPS, and TMBS rectifiers, as well as normally-OFF vertical GaN power transistors, including GaN CAVETs, GaN JFETs, GaN MOSFETs, and GaN FinFETs. However, the fabrication technologies for these GaN devices are still being developed and far from mature, especially in ion implantation, etching, and selective area doping processes, and the associated device performance could be further improved.

Among all the fabrication processes, selective area doping is one of the most critical ones. It enables the laterally patterned p-n junction structure, which is essential to many of the abovementioned advanced GaN power devices. Currently, there are several routes toward realizing selective area doping in GaN. The goal is to produce arbitrarily placed, contacted, and generally useable p-n junctions. The first route is solid-state diffusion. It involves the deposition of Mg sources on GaN surface and thermal annealing to diffuse Mg into GaN. However, it faces challenges in surface degradation under high-temperature annealing, formation of compensating defects under high Mg incorporation, and Mg activation. The second route is neutron and photonuclear transmutation. This technology uses neutrons or high-energy gamma rays to convert Ga into Ge (n-type dopant) or Zn (p-type dopant). Although good n-type doping was achieved in GaN, p-type conductivity has not been realized yet. The third route is ion implantation, which is widely used in Si and SiC devices to realize selective area doping. Very high annealing temperatures are needed to activate Mg and recover implantation damage. However, GaN decomposes at relatively lower temperatures; therefore, surface decomposition is a serious challenge in the process. There is some progress in preventing GaN decomposition during annealing using multicycle rapid thermal annealing [51], [52], and ultrahigh pressure [53]–[55]. Mg activation ratio and hole mobility comparable to as-grown p-GaN have been realized. However, the equipment needed to carry out these novel thermal annealing processes is not readily accessible to researchers and companies in the field, which could hinder their widespread implementation. Approaches to decrease the required annealing temperatures and pressures will be highly desired. If a reliable, simple, accessible, and efficient p-type ion implantation can be developed for GaN, it will significantly facilitate the mass adoption of GaN power technology to compete with the more mature Si and SiC technologies.

The fourth route is selective area regrowth. Recently, regrown planar GaN p-n junctions exhibited promising performance with reduced leakage and increased breakdown voltages through etching optimization and proper surface treatment. In addition, low-leakage lateral p-n junctions still need significant research efforts since regrowth in trenches can be drastically different from the regrowth on planar surfaces. Comprehensive growth and materials investigations are needed to study the lateral p-n junctions, including growth dynamics, etching conditions, postetching treatments, dopant profiling, impurity control, electronic structures at the regrowth interface, and so on. One of the complexities of lateral p-n junctions is that both the lateral and vertical leakages have to be suppressed, where the basal c-plane and sidewall planes have very differ-

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ent properties. Another important direction of selective area doping and regrowth is developing novel etching methods to reduce etching damage. Currently, there are some reports on ALE [74], [75], *in situ* etching [70], and photoelectrochemical (PEC) wet etching [76]. Their effects on device performance remain to be seen. With the progress of selective area doping in GaN, more advanced devices should be demonstrated, even the insulated-gate bipolar transistors (IGBTs). Finally, failure analysis and reliability study of vertical GaN power devices are also critical in increasing the maturity and wider adoption of this technology.

The research and development on vertical GaN devices have seen remarkable progress, from device conceptions, fabrication technologies, to prototype demonstrations, as discussed in this review. These exciting results are enabled by a close interaction between interdisciplinary fields, such as materials epitaxy sciences, material characterizations, semiconductor fabrication technologies, and semiconductor power devices, which may eventually lead to the maturity and wide adoption of vertical GaN power device technology. A revolution in the power electronics technology will bring about a fundamental change in how we can convert, distribute, control, and utilize electricity and revolutionize the power grid for the 21st century.

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