GaN Ring Oscillators Operational at 500 °C Based on a GaN-on-Si Platform

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***Abstract*— A study of GaN for high temperature (HT, up to 500 °C) digital circuits was conducted. A HT-robust GaN-on-Si technology based on enhancement-mode p-GaN-gate AlGaN/GaN high electron mobility transistors (HEMTs) and depletion-mode AlGaN/GaN HEMTs was proposed and used to implement different digital circuit configurations, namely E/D-mode and E/E-mode (E: enhancement, D: depletion). The E/D-mode inverter was found to offer significantly better performance in terms of voltage swing, noise margin, and gain, across temperature and V_{DD} scaling. As calculated from E/D-mode ring oscillators (ROs) with $L_G = 2$ μm, a RO exhibited a propagation delay (t_p) of < 1.48 ns/stage at 500 °C. The best RO achieved t_p < 0.18 ns/stage at 25 °C. To the best of the authors' knowledge, the proposed technology sets a new boundary of t_p *vs.* L_G in wide band gap digital logic, and is operational at the highest reported temperature (500 °C) of a GaN digital circuit. The results reflect the promising potential of the proposed technology for emerging HT applications at 500 °C and beyond.**

***Index Terms*— GaN, p-GaN-gate, transistor, high temperature, E/D-mode, E/E-mode, ring oscillator, propagation delay.**

I. Introduction

EMERGING applications such as deep well oil drilling, hypersonic aircrafts, and exploration of Venus require high temperature (HT)-rated electronics components beyond the Si technology's typical temperature limit of 250 °C [1], [2]. Wide band gap semiconductors (SiC and GaN) are well suited to meet this demand thanks to their wide band gap and negligible carrier thermal generation at these temperatures [3]. While SiC HT digital circuits based on several transistor types have been proposed [4], [5], [6], [7], GaN and III-N materials offer significant advantages in a *wider* range of applications from power [8], [9], [10] and RF [11], [12], [13], to MEMS [14], [15] and digital circuits [16], [17] across a large range of temperatures (from deep cryogenic temperature of 4 K to HT > 1000 °C). In spite of these opportunities, their use in HT digital and analog circuits remains a relatively unexplored area.

For GaN digital circuits, an Enhancement-mode (E-mode) transistor is highly desired to avoid the need of an additional negative voltage supply (V_{SS}) [18]. This E-mode transistor could be realized using a number of technology options, including, (1) F-plasma treatment of gate region [19]; (2) recessed MIS gate [20]; (3) FinFET [21]; (4) p-GaN-gate [22]. Among these, the p-GaN-gate is especially interesting for HT robust operation thanks to the lack of gate dielectric (which degrades at HT and may introduce traps at the dielectric/semiconductor interface), and simplicity in process flow. Furthermore, at the technology platform level, the p-GaN-gate AlGaN/GaN HEMT offers the possibility of monolithic integration with both depletion-mode (D-mode) n-FETs ([23], [24]) and E-mode p-FETs ([16], [17], [25], [26]).

In this work, HT digital circuits were realized based on p-GaN-gate AlGaN/GaN HEMTs which are optimized for HT operation and have been demonstrated to offer robust performance at least up to 500 °C [27]. The DC (static) performance of inverters with two different circuit configurations (E/D-mode and E/E-mode) was studied. Based on the results at the inverter-level, ring oscillators (ROs) were demonstrated in order to understand the propagation delay (t_p), an important performance metric for HT digital circuits.

II. Choice of Inverter Circuit Configuration

As illustrated in Fig. 1(a), the wafer platform used in this work is p-GaN/AlGaN/GaN-on-Si and allows for the monolithic integration of two types of transistors, E-mode p-GaN-gate AlGaN/GaN HEMTs and D-mode AlGaN/GaN HEMTs, using the process flow described in [28]. Here, HT transistors with refractory metal gate and self-alignment in p-GaN-gate were fabricated. The typical transfer characteristics of the E-mode and D-mode transistors ($L_G = L_{GS} = L_{GD} = 2$ μm) are shown in Fig. 1(b). Good ON-OFF ratio (> 3×10^7, limited by gate leakage) and V_{th} of 1.4 V at room temperature are obtained for the E-mode transistors. The D-mode transistor shows a V_{th} of −1 V.

In order to identify the optimal implementation of the GaN high temperature logic, the characteristics of two classic inverter configurations (E/D-mode and E/E-mode inverters) (Fig. 1(c)) were experimentally evaluated at high temperature.

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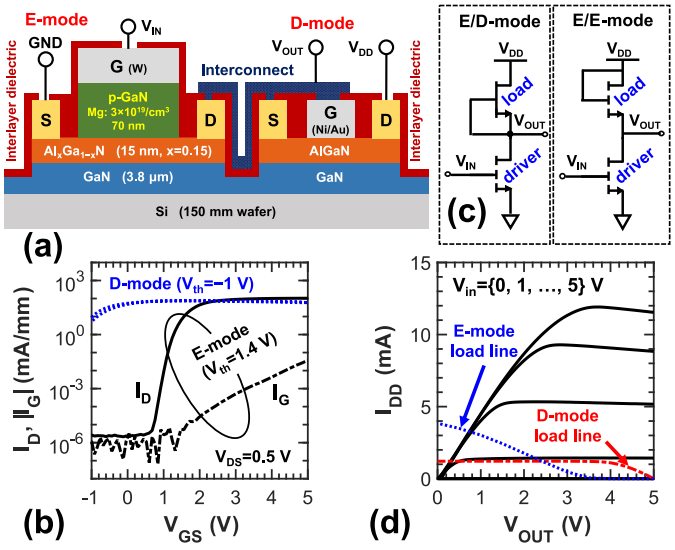

Fig. 1. Transistor technology and circuit configurations of *n*-FET only logic. (a) Illustration of the E-mode transistor (p-GaN-gate AlGaN/GaN HEMT) and D-mode transistor (AlGaN/GaN HEMT) connected as an E/D-mode inverter. In all transistors, $L_G = L_{GS} = L_{GD} = 2\ \mu$m. (b) Typical transfer characteristics of the E-mode and D-mode transistors. (c) Circuit configurations of E/D-mode and E/E-mode logic. (d) IV curves of an E-mode transistor ($W/L = 36/2\ \mu$m/μm). $I_{D,max} = 330$ mA/mm, $R_{ON} = 12\ \Omega$·mm (measured at $V_{GS} = 5$ V). The load line, realized using a either D-mode or E-mode transistor ($W/L = 12/2\ \mu$m/μm), is also included. The above measurements are conducted at room temperature.

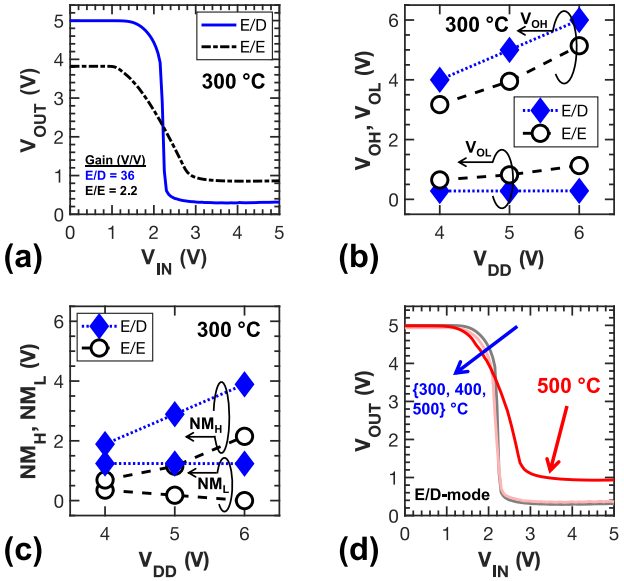

Fig. 2. Comparison of E/D-mode and E/E-mode inverters. (a) VTC at 300 °C. Maximum voltage gains of E/D-mode and E/E-mode are 36 V/V (at $V_{in} = 2.1$ V) and 2.2 V/V (at $V_{in} = 2.6$ V), respectively. (b) V_{OH}, V_{OL} *vs.* V_{DD} for E/D-mode and E/E-mode at 300 °C. V_{swing} may be calculated by $V_{OH} - V_{OL}$. (c) Noise margins (NM_L, NM_H) *vs.* V_{DD} for E/D-mode and E/E-mode at 300 °C. (d) VTC of E/D-mode up to 500 °C.

In principle, the E/E-mode inverter offers: (1) higher simplicity, (2) higher current, and (3) higher speed at higher V_{DD}, while the E/D inverter features (1) lower power consumption, (2) better gain, voltage swing (V_{swing}), and noise margin (NM), and (3) higher speed at lower V_{DD}, based on basic digital circuit theory and the prior work in other semiconductor technologies [29]. In the inverters of this work, the driver and load transistors are set to $W/L = 36/2\ \mu$m/μm and $12/2\ \mu$m/μm, respectively. The transistor sizing is determined based on: (1) the characteristics of the load line (Fig. 1(d)), (2) trade-offs between symmetricity in the DC (static) and transient (dynamic) characteristics of the inverter, (3) tolerance to non-uniformity and temperature variation in transistor characteristics, and (4) layout area. For a fair comparison between E/D-mode and E/E-mode, the same sizing is used.

A comparison of the voltage transfer curves (VTCs, Fig. 2(a)) at 300 °C reveals that, the E/D-mode inverter features significantly better performance than the E/E-mode inverter, in terms of V_{swing} ($= V_{OH} - V_{OL}$), gain, and NM. This is because: (1) In E/D-mode, $V_{OH} = V_{DD}$, whereas in E/E-mode, $V_{OH} = V_{DD} - V_{th(E)}$; (2) In both circuit configurations, V_{OL} is limited by the voltage drop across the E-mode driver. While the R_{ON} of both drivers is similar, the current drive of the E-mode load (diode-connected), when input is HIGH, is significantly stronger than that of the D-mode load (GS-tied) (Fig. 1(d)).

The above observations are also valid with the scaling of V_{DD}, an important design parameter in digital circuits (Fig. 2(b)–(c)). With the increase in V_{DD}, the V_{swing} of E/D-mode and E/E-mode inverters generally improves. However, the magnitude of improvement is better for the E/D-mode, thanks to the constant V_{OL} across different V_{DD}. When the output is LOW, the R_{ON} of the E-mode driver is almost independent of V_{DD} (Fig. 1(d)). To first order, the D-mode load supplies a constant current, compared to the current of E-mode load with V_{DD}^2 dependency, leading to a better V_{OL} at higher V_{DD}.

Having established that E/D-mode technology offers significantly better performance in GaN digital circuits at 300 °C, the temperature dependence of E/D-mode was further studied for higher temperatures. Measurements beyond 300 °C were conducted using a probe station with a hot chuck (maximum rating of 500 °C) and sealed chamber in N_2 ambient. As presented in Fig. 2(d), the VTC of the E/D-mode remains largely constant up till 400 °C, though NM_L is reduced slightly (by ~0.15 V) due to the faster degradation in the ON-resistance of the E-mode driver transistor than in the D-mode load transistor. At 500 °C, an increase in V_{OL} (hence reduction of V_{swing} by 0.6 V_{PP}) was observed, which can also be explained by the faster degradation of the E-mode device ON-resistance.

III. High Temperature Ring Oscillator and Propagation Delay

In order to estimate the t_p of the proposed GaN E/D-mode technology, ROs were fabricated with $(W/L)_{\{E,D\}} = \{36/2, 12/2\}\ \mu$m/$\mu$m (Fig. 3(a)). t_p was calculated by $T_{RO}/2N_{RO}$, where T_{RO} is the period of the RO waveform V_{OUT}, N_{RO} is the number of stages of the RO. The V_{DD} scaling trends of ROs were compared at 300 °C (Fig. 3(b)). The t_p may be modeled as $\frac{1}{2}C_L \times V_{DD}/I_{ave}$, where C_L is the load capacitance, and I_{ave} is the average charge/discharge current. To first order, the charge current through the D-mode load is constant with V_{DD} (refer to Fig. 1(d)), therefore t_p from LOW to HIGH (t_{pLH}) is proportional to V_{DD}. The discharge current through the E-mode driver, same as Si CMOS circuits, is roughly proportional to V_{DD}^2, therefore $t_{pHL} \propto 1/V_{DD}$.

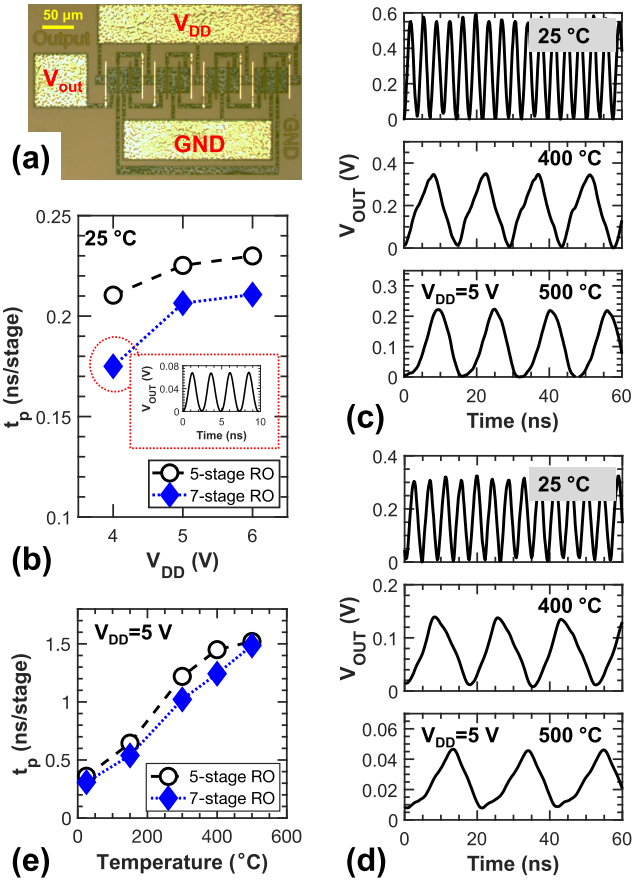

Fig. 3. GaN ring oscillators (ROs). (a) Micrograph of a 7-stage RO. (b) V_{DD} scaling trend of the best 5-stage RO and 7-stage RO at 25 °C. The inset presents the output waveform V_{OUT} of the 7-stage RO which demonstrates the best $t_p < 0.18$ ns/stage in this work. (c) Waveforms of another 5-stage RO at various temperatures. (d) Waveforms of another 7-stage RO at various temperatures. (e) t_p *vs.* temperature, estimated from the data reported in (c)–(d).

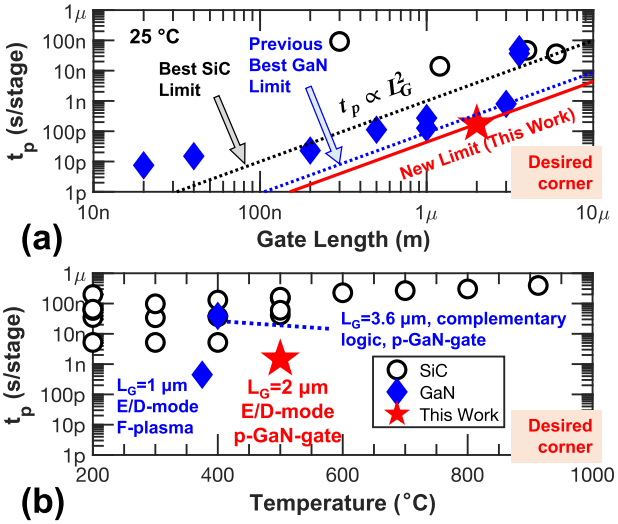

Fig. 4. A summary of ROs reported in the literature based on wide band gap electronics (GaN [17], [19], [22], [30], [31], [32], [33] and SiC [4], [5], [6], [7]). (a) t_p *vs.* L_G. The general scaling trends ($t_p \propto L_G^2$) for the best SiC demonstration, previous best GaN demonstration and the best result of this work (Fig. 3(b) inset) are included for reference. The L_G of the pull-down transistor is chosen. (b) t_p *vs.* temperature. The data points showing GaN RO demonstrations are labelled with the L_G of the pull-down transistor, the logic family/circuit configuration and the type of E-mode n-FET. To the best of the authors' knowledge, the proposed technology in this work defines a new boundary of t_p *vs.* L_G, as well as the operating temperature of GaN digital circuits.

Due to the significantly lower charge current, t_{pLH} dominates t_p. Hence, a lower V_{DD} results in a lower t_p. However, the reduction of V_{DD} results in trade-offs in NM and V_{swing} (Fig. 2(c)–(d)). Therefore, V_{DD} of 5 V was chosen for the RO as a compromise.

The ROs were operational at 500 °C, as shown in Fig. 3(c). The degradation of t_p from 0.31 ns/stage (25 °C) to 1.48 ns/stage (500 °C) (Fig. 3(d)) may be attributed to the performance degradation of both E/D-mode transistors (increase in R_{ON} of the E-mode driver, reduction in current drive capability of the D-mode load) and an increase in parasitics.

The best RO of this work ($t_p < 0.18$ ns/stage, Fig. 3(b) inset) was benchmarked against other ROs based on wide band gap electronics (GaN [17], [19], [22], [30], [31], [32], [33] and SiC [4], [5], [6], [7]). As shown in Fig. 4(a), to the best of the authors' knowledge, at room temperature, the proposed technology sets a new boundary in the well-known relationship of t_p *vs.* L_G^2 [34]. Furthermore, as shown in Fig. 4(b), the reported RO is operational at the highest reported temperature (500 °C) of a GaN digital circuit. The results reflect the promising potential of the proposed technology, which is based on p-GaN-gate AlGaN/GaN HEMTs optimized for HT ($\geq$ 500 °C) applications.

The measured values of t_p should be considered as an upper limit for the intrinsic t_p. As verified in Fig. 3(d), ROs with more stages would give a more accurate estimation of the intrinsic t_p. In the RO, in addition to the odd number of inverters connected in a circular chain, an output buffer is used for the readout of the output waveform (V_{OUT}). This buffer stage introduces a fixed delay whose relative contribution decreases as the number of stages increases. In this experiment, the number of stages in the E/D-mode RO was limited by the uniformity and yield of the fabrication. On the other hand, for E/E-mode ROs, the number of stages is limited by the low gain and low noise margins (especially NM_L) of each E/E-mode inverter stage (Fig. 2(a)), which makes the oscillations extremely difficult at high temperature.

IV. Conclusion

A study of E/D-mode and E/E-mode inverters realized by HT-optimized E-mode p-GaN-gate HEMT technology based on a GaN-on-Si platform was conducted. E/D-mode inverters were found to offer significantly higher performance than E/E-mode inverters at 300 °C. The reported RO exhibited a t_p of $<$ 1.48 ns/stage at 500 °C. The best RO achieved $t_p <$ 0.18 ns/stage at 25 °C with $L_G = 2$ μm. Further advancement of the proposed technology, e.g. optimization of the epitaxial structure, reduction of layout parasitics, and introduction of HT-rated advanced packaging [35], could significantly push the performance limit of GaN HT electronics.

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REFERENCES

[1] S. R. Eisner, H. S. Alpert, C. A. Chapin, A. S. Yalamarthy, P. F. Satterthwaite, A. Nasiri, S. Port, S. Ang, and D. G. Senesky, "Extended exposure of gallium nitride heterostructure devices to a simulated Venus environment," in *Proc. IEEE Aerosp. Conf.*, Mar. 2021, pp. 1–12, doi: 10.1109/AERO50100.2021.9438131.

[2] K. H. Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, "Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects," *J. Appl. Phys.*, vol. 130, no. 16, Oct. 2021, Art. no. 160902, doi: 10.1063/5.0061555.

[3] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics—A role for wide bandgap semiconductors?" *Proc. IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002, doi: 10.1109/JPROC.2002.1021571.

[4] U. Schmid, S. T. Sheppard, and W. Wondrak, "High temperature performance of NMOS integrated inverters and ring oscillators in 6H-SiC," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 687–691, Apr. 2000, doi: 10.1109/16.830980.

[5] J. Holmes, A. M. Francis, I. Getreu, M. Barlow, A. Abbasi, and H. A. Mantooth, "Extended high-temperature operation of silicon carbide CMOS circuits for Venus surface application," *J. Microelectron. Electron. Packag.*, vol. 13, no. 4, pp. 143–154, 2016, doi: 10.4071/imaps.527.

[6] P. G. Neudeck, D. J. Spry, L. Chen, N. F. Prokop, and M. J. Krasowski, "Demonstration of 4H-SiC digital integrated circuits above 800°C," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1082–1085, Aug. 2017, doi: 10.1109/LED.2017.2719280.

[7] M. Shakir, S. Hou, B. G. Malm, M. Östling, and C.-M. Zetterling, "A 600°C TTL-based 11-stage ring oscillator in bipolar silicon carbide technology," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1540–1543, Oct. 2018.

[8] J. Liu, M. Xiao, R. Zhang, S. Pidaparthi, H. Cui, A. Edwards, M. Craven, L. Baubutr, C. Drowley, and Y. Zhang, "1.2-kV vertical GaN fin-JFETs: High-temperature characteristics and avalanche capability," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 2025–2032, Apr. 2021, doi: 10.1109/TED.2021.3059192.

[9] L. Nela, N. Perera, C. Erine, and E. Matioli, "Performance of GaN power devices for cryogenic applications down to 4.2 K," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, Jul. 2021, doi: 10.1109/TPEL.2020.3047466.

[10] M. Sadek, S.-W. Han, J. Song, J. C. Gallagher, T. J. Anderson, and R. Chu, "High-temperature static and dynamic characteristics of 4.2-kV GaN super-heterojunction p-n diodes," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 1912–1917, Apr. 2022, doi: 10.1109/TED.2022.3149453.

[11] D. Maier, M. Alomari, N. Grandjean, J.-F. Carlin, M.-A. Diforte-Poisson, C. Dua, S. Delage, and E. Kohn, "InAlN/GaN HEMTs for operation in the 1000°C regime: A first experiment," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 985–987, Jul. 2012, doi: 10.1109/LED.2012.2196972.

[12] Q. Xie, N. Chowdhury, A. Zubair, M. S. Lozano, J. Lemettinen, M. Colangelo, O. Medeiros, I. Charaev, K. K. Berggren, P. Gumann, D. Pfeiffer, and T. Palacios, "NbN-gated GaN transistor technology for applications in quantum computing systems," in *Proc. Symp. VLSI Technol.*, Jun. 2021, p. T10-3.

[13] P. Palacios, T. Zweipfennig, A. Ottaviani, M. Saeed, C. Beckmann, M. Alomari, G. Lukens, H. Kalisch, J. N. Burghartz, A. Vescan, and R. Negra, "3D integrated 300°C tunable RF oscillator exploiting AlGaN/GaN HEMT for high temperature applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 519–522, doi: 10.1109/IMS19712.2021.9574881.

[14] Q. Xie, N. Wang, C. Sun, A. B. Randles, P. Singh, X. Zhang, and Y. Gu, "Effectiveness of oxide trench array as a passive temperature compensation structure in AlN-on-silicon micromechanical resonators," *Appl. Phys. Lett.*, vol. 110, no. 8, Feb. 2017, Art. no. 083501, doi: 10.1063/1.4976808.

[15] W. Chen, W. Jia, Y. Xiao, Z. Feng, and G. Wu, "A temperature-stable and low impedance piezoelectric MEMS resonator for drop-in replacement of quartz crystals," *IEEE Electron Device Lett.*, vol. 42, no. 9, pp. 1382–1385, Sep. 2021, doi: 10.1109/LED.2021.3094319.

[16] N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, "Regrowth-free GaN-based complementary logic on a Si substrate," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 820–823, Jun. 2020, doi: 10.1109/LED.2020.2987003.

[17] L. Zhang, Z. Zheng, Y. Cheng, Y. H. Ng, S. Feng, W. Song, T. Chen, and K. J. Chen, "SiN/*in-situ*-GaON staggered gate stack on p-GaN for enhanced stability in buried-channel GaN p-FETs," in *IEDM Tech. Dig.*, Dec. 2021, pp. 5.3.1–5.3.4, doi: 10.1109/IEDM19574.2021.9720653.

[18] A. Hassan, J.-P. Noël, Y. Savaria, and M. Sawan, "Circuit techniques in GaN technology for high-temperature environments," *Electronics*, vol. 11, no. 1, p. 42, Dec. 2021, doi: 10.3390/electronics11010042.

[19] Y. Cai, Z. Cheng, Z. Yang, C. W. Tang, K. M. Lau, and K. J. Chen, "High-temperature operation of AlGaN/GaN HEMTs direct-coupled FET logic (DCFL) integrated circuits," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 328–331, May 2007, doi: 10.1109/LED.2007.895391.

[20] J. He, Q. Wang, G. Zhou, W. Li, Y. Jiang, Z. Qiao, C. Tang, G. Li, and H. Yu, "Normally-OFF AlGaN/GaN MIS-HEMTs with low R_{ON} and V_{th} hysteresis by functioning *in-situ* SiN_x in regrowth process," *IEEE Electron Device Lett.*, vol. 43, no. 4, pp. 529–532, Apr. 2022, doi: 10.1109/LED.2022.3149943.

[21] Y. Zhang, A. Zubair, Z. Liu, M. Xiao, J. Perozek, Y. Ma, and T. Palacios, "GaN FinFETs and trigate devices for power and RF applications: Review and perspective," *Semicond. Sci. Technol.*, vol. 36, no. 5, Mar. 2021, Art. no. 054001, doi: 10.1088/1361-6641/abde17.

[22] J. Wei, G. Tang, R. Xie, and K. J. Chen, "GaN power IC technology on p-GaN gate HEMT platform," *Jpn. J. Appl. Phys.*, vol. 59, no. SG, Feb. 2020, Art. no. SG0801, doi: 10.7567/1347-4065/ab5b63.

[23] X. Li, S. Stoffels, B. Bakeroot, D. Wellekens, B. Vanhove, T. Cosnier, R. Langer, D. Marcon, G. Groeseneken, S. Decoutere, N. Amirifar, K. Geens, M. Zhao, W. Guo, H. Liang, S. You, N. Posthuma, and B. D. Jaeger, "GaN-on-SOI: Monolithically integrated all-GaN ICs for power conversion," in *IEDM Tech. Dig.*, Dec. 2019, pp. 4.4.1–4.4.4, doi: 10.1109/IEDM19573.2019.8993572.

[24] G. Lyu, J. Wei, W. Song, Z. Zheng, L. Zhang, J. Zhang, S. Feng, and K. J. Chen, "GaN on engineered bulk Si (GaN-on-EBUS) substrate for monolithic integration of high-/low-side switches in bridge circuits," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4162–4169, Aug. 2022, doi: 10.1109/TED.2022.3178361.

[25] J. Chen, Z. Liu, H. Wang, Y. He, X. Zhu, J. Ning, J. Zhang, and Y. Hao, "A GaN complementary FET inverter with excellent noise margins monolithically integrated with power gate-injection HEMTs," *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 51–56, Jan. 2022, doi: 10.1109/TED.2021.3126267.

[26] N. Chowdhury, Q. Xie, and T. Palacios, "Self-aligned E-mode GaN *p*-channel FinFET with $I_{ON} > 100$ mA/mm and $I_{ON}/I_{OFF} > 10^7$," *IEEE Electron Device Lett.*, vol. 43, no. 3, pp. 358–361, Mar. 2022, doi: 10.1109/LED.2022.3140281.

[27] M. Yuan, Q. Xie, J. Niroula, M. F. Isamotu, J. A. Greer, N. S. Rajput, N. Chowdhury, and T. Palacios, "High temperature robustness of enhancement-mode p-GaN-gated AlGaN/GaN HEMT," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2022.

[28] M. Yuan, "GaN electronics for high-temperature applications," M.S. thesis, Massachusetts Inst. Technol., Cambridge, MA, USA, Feb. 2020. [Online]. Available: https://hdl.handle.net/1721.1/128350

[29] X. Yanyang, Z. Xiaoguang, and H. Jingchen, "Direct coupled FET logic (DCFL) circuit for GaAs LSIC application," in *Proc. Int. Conf. Microw. Millim. Wave Technol.*, 1998, pp. 913–916, doi: 10.1109/ICMMT.1998.768438.

[30] A. L. Corrion, K. Shinohara, D. Regan, Y. Tang, D. Brown, J. F. Robinson, H. H. Fung, A. Schmitz, D. Le, S. J. Kim, T. C. Oh, and M. Micovic, "High-speed 501-stage DCFL GaN ring oscillator circuits," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 846–848, Jul. 2013, doi: 10.1109/LED.2013.2264796.

[31] Y. Kong, J. Zhou, C. Kong, Y. Zhang, X. Dong, H. Lu, T. Chen, and N. Yang, "Monolithic integration of E/D-mode AlGaN/GaN MIS-HEMTs," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 336–338, Mar. 2014, doi: 10.1109/LED.2013.2297433.

[32] R. Hao, C. Sun, B. Fang, N. Xu, Z. Tao, H. Zhang, X. Wei, W. Lin, X. Zhang, G. Yu, Z. Zeng, Y. Cai, X. Zhang, and B. Zhang, "Monolithic integration of enhancement/depletion-mode high electron mobility transistors using hydrogen plasma treatment," *Appl. Phys. Exp.*, vol. 12, no. 3, Feb. 2019, Art. no. 036502, doi: 10.7567/1882-0786/aafcd5.

[33] M. Micovic, T. Tsen, M. Hu, P. Hashimoto, P. Willadsen, I. Milosavljevic, A. Schmitz, M. Antcliffe, D. Zhender, and J. Moon, "GaN enhancement/depletion-mode FET logic for mixed signal applications," *Electron. Lett.*, vol. 41, no. 19, pp. 1081–1083, Sep. 2005, doi: 10.1049/el:20052263.

[34] H. S. Momose, E. Morifuji, T. Yoshitomi, T. Ohguro, M. Saito, and H. Iwai, "Cutoff frequency and propagation delay time of 1.5-nm gate oxide CMOS," *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1165–1174, Jun. 2001, doi: 10.1109/16.925243.

[35] F. Li and S. Raveendran, "Wirebonding based 3-D SiC IC stacks for high temperature applications," in *Proc. IEEE 72nd Electron. Compon. Technol. Conf. (ECTC)*, May 2022, pp. 2023–2027, doi: 10.1109/ECTC51906.2022.00319.