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ORIGINAL RESEARCH ARTICLE

Impact of Substrate Morphology and Structural Defects in Freestanding Gallium Nitride on the Breakdown Characteristics of GaN-on-GaN Vertical Diodes

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Abstract

The morphology of GaN substrates grown by hydride vapor-phase epitaxy (HVPE) and by ammonothermal methods has been correlated with reverse-bias stress testing applied to GaN-on-GaN *p-i-n* diodes. GaN substrates grown by HVPE showed ordered, well-separated arrays of surface features when observed using x-ray topography (XRT). All fabricated diodes that overlapped with these features had reverse-bias voltages typically of less than 100 V before reaching a critical leakage current limit that was set at 10^{-6} A. In contrast, diodes not overlapping with such features reached reverse-bias voltages exceeding 300 V for the same leakage current limit. After surface etching, the HVPE substrate showed evidence for defect clusters and macro-pits. XRT images of the ammonothermal GaN substrate revealed no visible features. However, some diodes fabricated on the ammonothermal substrate still failed to reach reverse-bias voltages comparable to those of the HVPE-grown samples. Diodes on HVPE and ammonothermal substrates with low breakdown voltage showed crater-like surface damage. Progressive ion milling across such failed devices revealed the presence of voids and threading dislocations that penetrated deep into the substrate (~ 25 µm); these features were not observed in diodes with high reverse-bias voltages and low leakage current. This work emphasizes the potential unsuspected impact of substrate morphology in limiting the performance of vertical GaN devices.

Keywords GaN · freestanding substrates · hydride vapor-phase epitaxy · ammonothermal · vertical *p-n* diodes

Introduction

Semiconductor devices based on GaN are of special interest for high-power applications because of their enhanced properties in comparison with traditional Si-based devices. GaN has a wide bandgap (3.44 eV), high critical electric field (~ 10 × Si), low intrinsic carrier concentration, high thermal conductivity (~ 1.5 × Si), and high saturation velocity (~ 3 × Si).[1–5] Vertical GaN devices are preferred to lateral devices because of reduced die size, improved reliability, and higher efficiency, while the growth of thicker epitaxial layers enables high-current and high-voltage applications.[6,7]

Earlier generations of GaN devices grown on common substrates, such as Si, SiC, and sapphire, had very high defect densities (10^8–10^{10} cm^{-2}), primarily due to the large lattice mismatch between materials.[8] The high density of threading dislocations (TDs) contributes to non-radiative recombination and scattering centers that eventually limit device performance.[9] Since such defects can affect breakdown voltage, leakage current, device reliability, high-temperature reverse bias, and operating lifetime, it is critical to minimize defect densities.[10] Freestanding GaN substrates with defect densities of less than ~ 10^6 cm^{-2} have become available due to developments in hydride vapor pressure epitaxy (HVPE) and ammonothermal growth methods.[11] Epitaxial GaN-on-GaN layers can be grown with even lower

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defect density ($< 10^4$ cm^{-2}) using these bulk substrates, in turn making it feasible to fabricate high-power GaN-on-GaN vertical devices with high breakdown voltages.[12]

Although these developments in growth techniques have led to bulk GaN substrates with substantially less defects, the presence of random and unavoidable defects can still lead to degraded device performance and eventual device failure. For example, it is well known that TDs are the most likely reason for leakage current in GaN-based devices.[13,14,41] These TDs can act as trap centers due to the presence of metastable acceptor- and donor-like states in the vicinity of the defects.[15,16] Increased leakage current has been reported in GaN-based devices grown by several methods, including molecular beam epitaxy,[17,18] metal–organic vapor-phase epitaxy,[19,20] and HVPE.[21] Two recent studies also noted the important role of dislocations in affecting performance of almost all types of GaN-based devices.[39,40] Since defects cannot be avoided altogether, device fabrication should be concentrated where possible in areas with minimized defect densities, rather than areas having large defect concentrations, in order to avoid defect-related current leakage and possible device breakdown.

It has been reported that HVPE-grown GaN substrates with extensive regions of low dislocation density ($\sim 10^5$ cm^{-2}) could be obtained by deliberately concentrating the dislocations around pits with predetermined locations.[22] Another report suggested that the selective growth of GaN by HVPE, through openings in an SiO_2 mask, likewise reduced the dislocation density (TDs $\sim 10^7$ cm^{-2}) in overgrown layers.[23] One study reported that bulk GaN grown by HVPE achieved a low etch-pit density (EPD) of $\sim 10^6$ cm^{-2} by removal of the base Si substrate at high temperature.[24] It was also reported that bulk GaN with "near-perfect" crystal quality (EPD of $\sim 3 \times 10^2$ cm^{-2}) could be obtained by HVPE GaN regrowth after the intentional formation of an ordered array of etch pits in the base GaN layer; it was stated that the etch pits transformed into voids after regrowth and thus did not propagate dislocations into the overgrown layers.[12] Another study reported bulk GaN grown by ammonothermal methods, again with low dislocation density ($< 10^6$ cm^{-2}).[25] More recent studies reported dislocation density as low as $< 5 \times 10^4$ cm^{-4} for GaN grown by using a combination of HVPE and ammonothermal techniques.[35,36] Recent study of metal–organic chemical vapor deposition (MOCVD)-grown GaN *p-n* fabricated on HVPE-grown GaN substrates observed that current leakage paths overlapped with TDs.[37] Another study reported that TDs impacted GaN-on-GaN device performance by acting as centers for localized carrier concentrations.[38] A further study of GaN switches with vertical and lateral structure fabricated on different types of substrates noted that TDs in the device carrier path lead to carrier scattering, charge trapping, and increased leakage current.[40]

Given these developments of bulk GaN substrates of high quality, there is much interest in determining whether the improved morphology of these substrates might positively impact subsequent device behavior. However, device performance can also be impacted by processing methods such as plasma etching for selective-area doping that are used to create complicated device structures, and edge-termination techniques such as hydrogen passivation.[26–28] Given the complexity of possible causes for degraded devices, identifying the specific reason(s) for device failure can often be challenging. This present work has investigated GaN-on-GaN vertical diodes that were grown on HVPE substrates originating from two different sources and one ammonothermal substrate.[29] In order to investigate the influence of the substrate and to avoid the interference of other factors, the design and processing of the devices was kept as consistent as possible. The fabricated devices were characterized by x-ray topography (XRT), scanning electron microscopy (SEM), and transmission electron microscopy (TEM), and the results have been correlated with electrical performance, as measured in terms of leakage current under reverse-bias conditions.

Materials and Methods

GaN substrates from three different sources, all with slight offcuts of ~ 0.4°–0.6° to encourage step-flow growth,[30] were used for device fabrication. The two grown by HVPE came from two different companies, which used different growth approaches and patterns to reduce the dislocation density in the GaN substrates,[31,32] and are labeled here as S-1 and S-2. The third substrate was grown by the ammonothermal method and is labeled here as S-3. These freestanding n^+-GaN substrates were 2-inch *c*-plane with thicknesses of ~ 330 µm and carrier concentrations of ~ 10^{18} cm^{-3}. Unintentionally doped (UID) GaN drift layers ($\sim 1 \times 10^{16}$ cm^{-3}) with thicknesses of ~ 2.2 µm were grown on all three GaN substrates by MOCVD, followed by growth of Mg-doped *p*-GaN layers ($\sim 1 \times 10^{19}$ cm^{-3}) with thicknesses of ~ 500 nm and p^+-GaN layers ($\sim 1 \times 10^{20}$ cm^{-3}) with thicknesses of ~ 20 nm. Atomic force microscopy measurements showed that the root mean square (rms) surface roughness of epilayers S-1, S-2, and S-3 were 0.79 nm, 1.08 nm, and 0.58 nm, respectively. Activation of the regrown *p*-GaN layers was carried out by rapid thermal annealing at 700 °C for 20 min in an N_2 environment. Diodes fabricated on each wafer had sizes ranging from 60 to 300 µm in diameter, and are identified later according to their size. A schematic of the device structures (not to scale) is shown in Fig. 1.

Metal stacks of Pd/Ni/Au (10 nm/20 nm/50 nm) for *p*-GaN ohmic contacts were deposited by electron-beam evaporation, followed by annealing at 450 °C for 5 min in

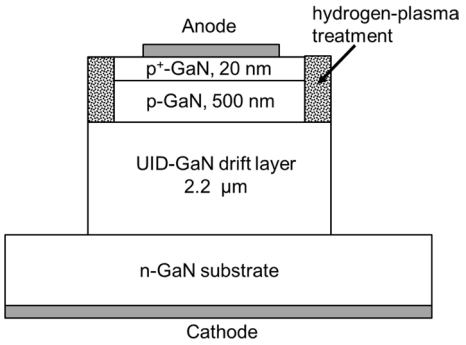

Fig. 1 Schematic showing fabricated *p-i-n* structure (not to scale).

N_2 ambient. Mesa isolation and hydrogen-plasma passivation were used for edge termination. Metal stacks of Ti/Al/Ni/Au (20 nm/130 nm/50 nm/150 nm) for ohmic contact were deposited by electron-beam evaporation on the backsides of the GaN substrates without annealing. Native surface oxides were removed before deposition of the metal contacts by cleaning with acetone/isopropyl alcohol, followed by hydrochloric acid. The PlasmaTherm Apex ICP chlorine-based tool, which is a load-locked, inductively coupled plasma (ICP) etch system, was used for etching. The ICP power and the radio-frequency (RF) power were 400 W and 70 W, respectively, and the BCl_3 flow rate, Cl_2 flow rate, and Ar flow rate were 8 sccm, 30 sccm, and 5 sccm, respectively, for an etch rate of ~ 288 nm/min.

Current–voltage (I–V) measurements (limited to a maximum of 1000 V) were made using a Keithley 2410 source-meter. The ramp rate (bias step) was 1 V, and the dwell time for each point was 100 ms. All of the fabricated diodes in this study had turn-on voltages of ~ 3.4 V, as measured from forward I–V characteristics. The reverse I–V characteristics of the diodes were compared with respect to a specific leakage current cutoff, which was set at 10^{-6} A in order to avoid irreversible device breakdown. Corresponding I–V curves for all diodes fabricated on each of the three wafers are shown plotted on a semi-log scale in Fig. 2. As indicated, the devices had a range of diameters from 60 μm to 300 μm, and are identified according to their size, such as "60–3" for the third device with 60-μm diameter.

XRT images of the various wafers were taken with a Rigaku XRT-100 operated at 50 kV voltage and 30 mA current. All XRT measurements were taken under reflection mode with a Cu $K_{\alpha 1}$ x-ray source. Samples suitable for cross-sectional TEM observation were prepared by focused-ion-beam (FIB) milling using a FEI Nova 200 dual-beam system, with initial thinning done at 30 keV and final thinning done at 5 keV to reduce the amount of ion-milling damage. Scanning electron micrographs were also recorded during the FIB milling process. A Philips-FEI CM-200 field-emission gun transmission electron microscope operated at 200 keV was used for structural imaging.

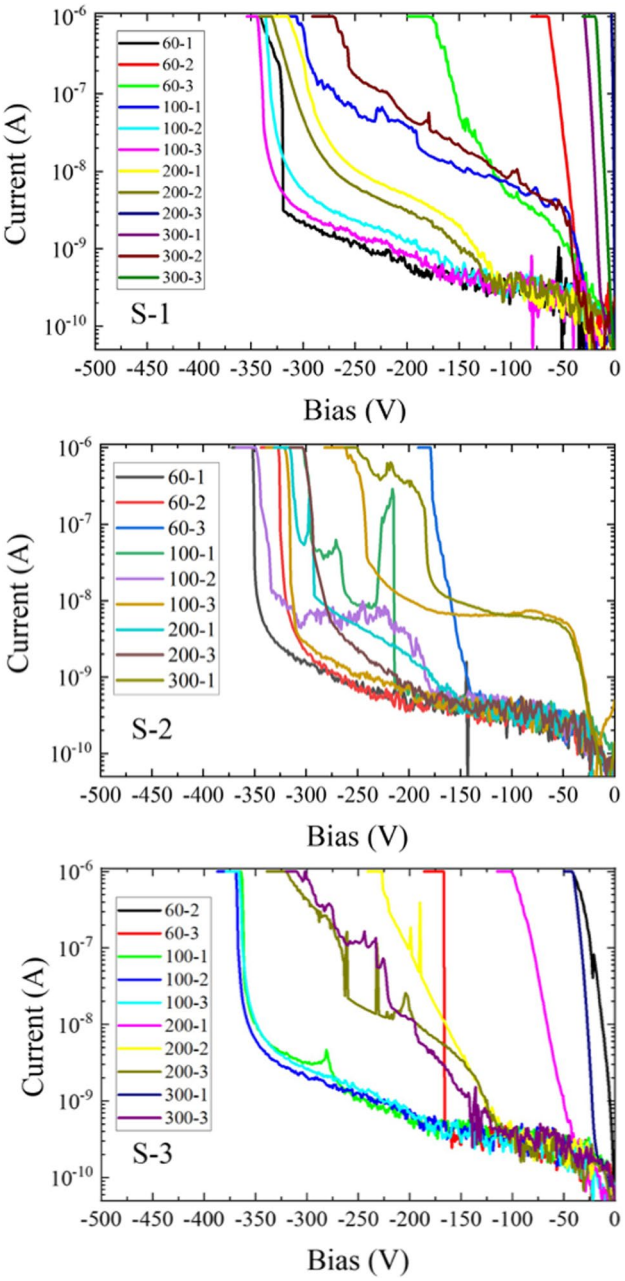

Fig. 2 Reverse-bias I–V curves for wafers S-1, S-2, and S-3, plotted on a semi-log scale, with current threshold current limit set at 10^{-6}A.

Results and Discussion

Table I lists the maximum voltage that was applied to each of the devices fabricated on Wafer S-1 before the current reached the set threshold of 10^{-6} A. The descriptors of "High" and "Low" are used to indicate devices that showed

Table I Summary of I–V measurements for Wafer S-1

60–1 High (−342 V)	100–1 High (−306 V)	200–1 High (−314 V)	300–1 Low (< −50 V)
60–2 Low (< −65 V)	100–2 High (−336 V)	200–2 High (−330 V)	300–2 Low (< −270 V)
60–3 Low (−179 V)	100–3 High (−344 V)	200–3 Low (< −50 V)	300–3 Low (< −50 V)

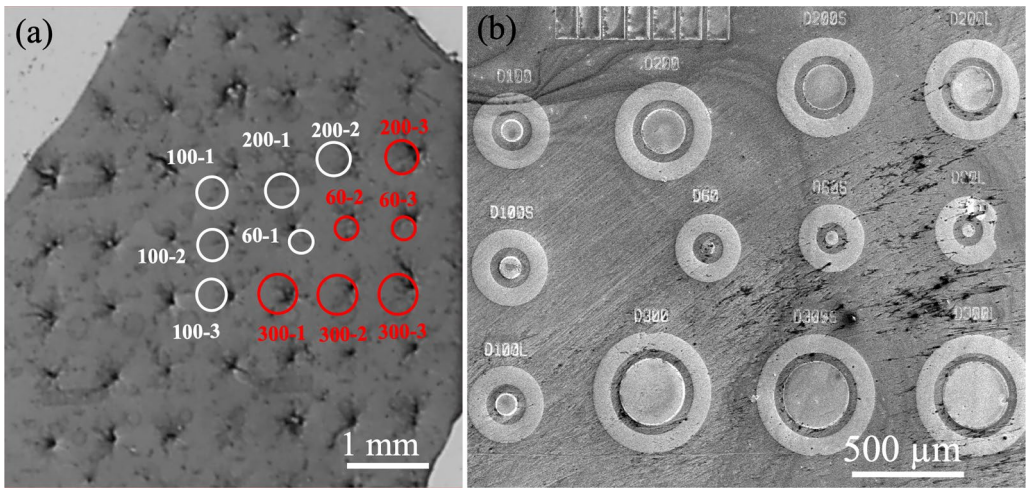

Fig. 3 (a) XRT image of HVPE-grown Wafer S-1 showing a two-dimensional array of dark spots with ~ 1 mm separation. Circles indicate locations where diodes were later fabricated. Red and white colors indicate devices showing low and high reverse-bias thresholds, respectively. (b) Low-magnification SEM image showing diodes fabricated at locations indicated in (a).

what were considered to be high or low reverse-bias breakdown voltage.

Figure 3a is an XRT image of Wafer S-1 that shows a two-dimensional array of dark spots, which are roughly equally spaced with separation distances of ~ 1 mm. These periodic arrays are attributed to the process used to gather dislocations during substrate growth.[33] All of the fabricated devices in locations marked by red circles reached the cut-off threshold for leakage current at relatively low reverse-bias voltages, whereas the devices in locations marked by white circles reached reverse-bias voltages of greater than 300 V. Figure 3b shows a low-magnification SEM image of the diodes fabricated at the locations circled in Fig. 3a. The correlation of these images with the corresponding device measurements in Table I shows that fabricated diodes that overlapped with the dark spots had low reverse-bias voltage limits and are thus considered to have performed poorly. In contrast, diodes in locations away from such regions had reverse-bias voltages exceeding 300 V before reaching the pre-specified leakage current threshold.

Figure 4 shows an XRT image of Wafer S-2, where the red and white circles again indicate the locations of fabricated diodes that showed low and high reverse-bias thresholds, respectively. Discontinuous, mostly vertical, features are visible that are roughly separated by ~ 1 mm. Table II shows a summary of the corresponding I–V measurements. Those fabricated in locations overlapping with the discontinuous, vertical features had excessive leakage current under relatively low reverse-bias voltage, whereas diodes located away from such features performed more robustly, again reaching reverse-bias voltages of greater than 300 V.

Figure 5 is an XRT image of Wafer S-3, which is the GaN-on-ammonothermal GaN substrate, with red and white circles again indicating the locations of fabricated diodes which showed low and high reverse-bias voltage limits, respectively. No noticeable morphology features are visible. However, diodes fabricated on this wafer did not perform consistently, as shown by the electrical results summarized in Table III. Some diodes reached high reverse-bias voltage limits exceeding 320 V without significant leakage, whereas some diodes only reached reverse-bias voltages in the range of 50–200 V before substantial leakage current started to occur.

In order to provide further insight into this dependence of device behavior on surface and subsurface features, two HVPE-grown wafers nominally similar to S-1 were etched and then observed by SEM. These two wafers, labeled here as S-A and S-B, were etched using ICP recipes with different RF power. Wafer S-A was etched with an RF power of 70 W for 2 min, which removed ~ 500 nm of the top surface layer, while Wafer S-B was etched with reduced RF power of 5 W for 2 min, which removed a surface layer of ~ 40 nm. Figure 6 shows XRT images of these two wafers before any

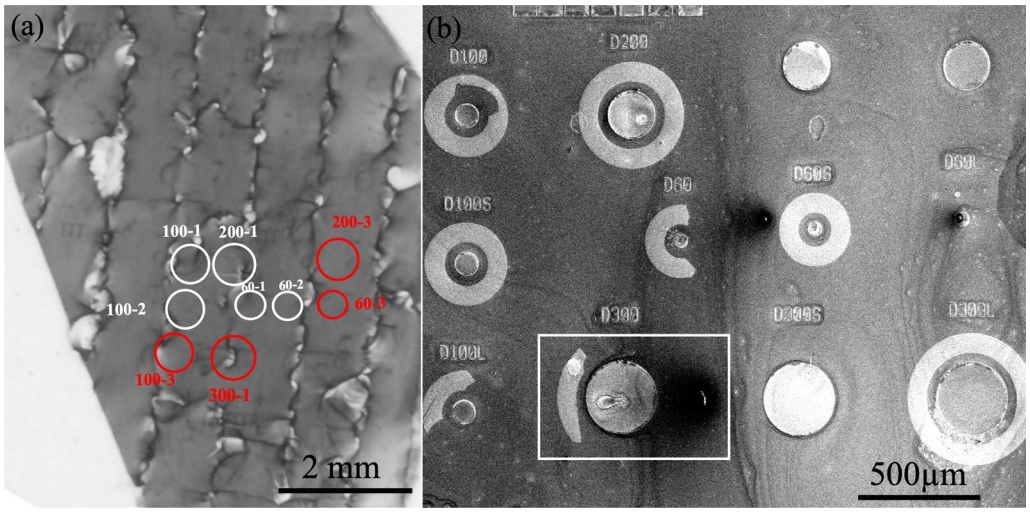

Fig. 4 (a) XRT image of HVPE-grown Wafer S-2 showing discontinuous and vertical features with lateral separation of roughly 1 mm. Circles indicate locations where diodes were later fabricated. (b) Low-magnification SEM image showing devices fabricated at locations indicated in (a). The device within the box was stress tested to breakdown (see Fig. 10).

Table II Summary of I–V measurements for Wafer S-2

60–1 High (−352 V)	100–1 High (−303 V)	200–1 High (−316 V)	300–1 Low (−250 V)
60–2 High (−327 V)	100–2 High (−350 V)	NA	NA
60–3 Low (−179 V)	100–3 High (−263 V)	200–3 High (−303 V)	NA

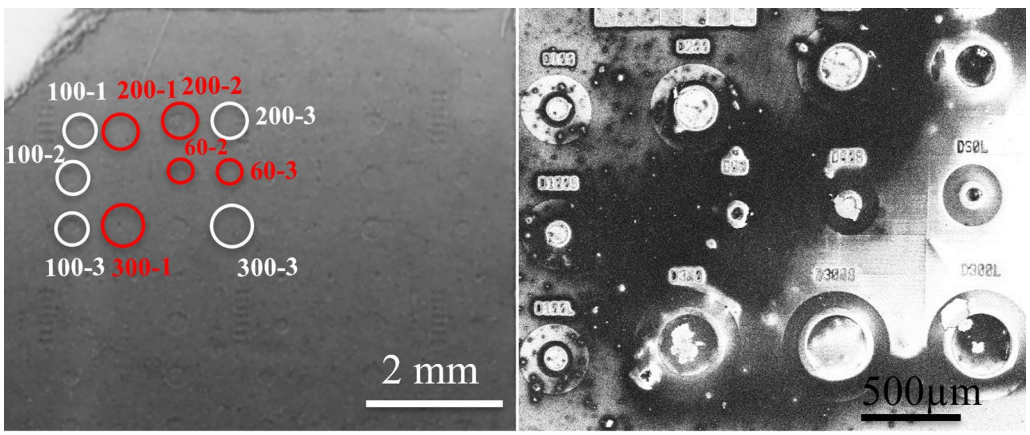

Fig. 5 (a) XRT image of Wafer S-3 as grown by the ammonothermal method. No macroscopic-sized features are visible. Circles indicate locations where diodes were later fabricated. (b) Low-magnification SEM image showing diodes fabricated at locations indicated in (a).

Table III Summary of I–V measurements for Wafer S-3

NA	100–1 High (−365 V)	200–1 Low (−101 V)	300–1 Low (−43 V)
60–2 Low (−43 V)	100–2 High (−370 V)	200–2 Low (−228 V)	NA
60–3 Low(−168 V)	100–3 High (−366 V)	200–3 High (−321 V)	300–3 High (−311 V)

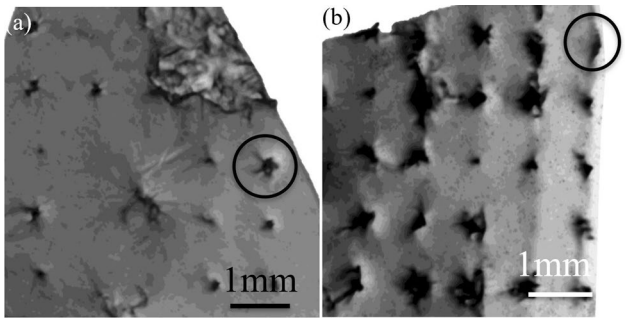

Fig. 6 XRT images before etching: (a) Wafer S-A and (b) Wafer S-B. SEM images of the circled regions after etching are shown in later figures.

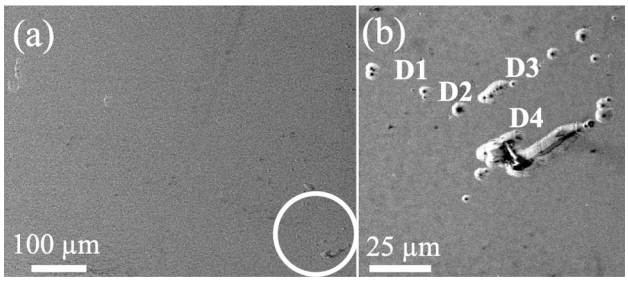

Fig. 7 (a) Plan-view SEM image of Wafer S-A showing the location marked by the circle in Fig. 6a. (b) Medium-magnification image showing a cluster of defects from the location marked in (a).

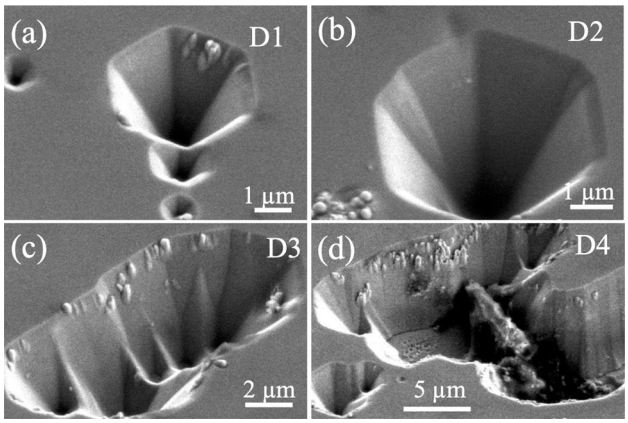

Fig. 8 Enlarged images of Wafer S-A showing the locations marked in Fig. 7b: (a) series of inverted-hexagonal pyramidal pits at location D1; (b) large pit with width ~ 5.5 µm at location D2; (c) several (~ 5–6) closely packed hexagonal pits; and (d) large, irregular-shaped pit likely formed by amalgamation of several smaller pits.

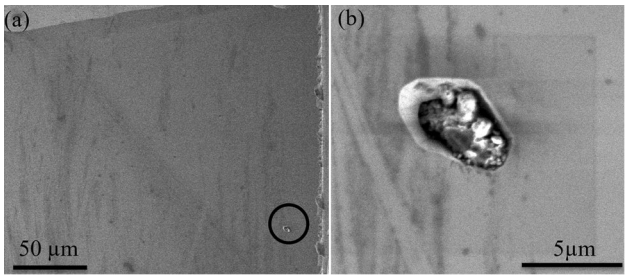

Fig. 9 Plan-view SEM images of Wafer S-B from the location circled in Fig. 6b: (a) low-magnification image showing no substantial surface features; (b) higher-magnification image showing an irregular surface pit at the location circled in (a).

etching was performed: The regions observed by SEM after etching are circled.

Figure 7 shows plan-view SEM images of Wafer S-A after etching at the location circled in Fig. 6a. Some surface features are faintly visible in Fig. 7a, but no large macroscopic-sized defect can be seen. Figure 7b shows a medium-magnification image of the area indicated by the box in Fig. 7a: A cluster of pits, labeled as D1, D2, D3, and D4, is visible. Figure 8 shows enlarged SEM images of these four regions. Figure 8a and b show inverted, hexagonal-shaped pyramidal pits of different sizes. Figure 8c shows a region with 5–6 closely packed hexagonal pits, and Fig. 8d shows a continuous and large defect, possibly formed by the amalgamation of several pits.

Figure 9 shows SEM images of Wafer S-B from the location circled in Fig. 6b. No noticeable features such as those visible in Fig. 8 can be seen. Clearly, the amount of etching has played an important role in exposing the apparent surface features observed in wafers by XRT. Thus, the faster (deeper) etching has helped in exposing significant subsurface features that are observed by XRT but are not revealed by the reduced (shallower) etching.

In order to better appreciate the possible role played by substrate defect morphology in diode failure, the device 60–2 on Wafer S-3, which suffered premature breakdown (< 50 V), was progressively milled in cross section *across* the visibly damaged surface, and then imaged in situ with the SEM after completion of each milling cycle. Figure 10a shows an SEM image of the device before commencement of trenching. The series of SEM images in Fig. 10b–g, each taken after another roughly 5 µm had been progressively milled away across the wafer surface, shows a significant density of threading dislocations that extend deep (~ 26 µm) into the substrate. Finally, Fig. 10h shows a plan-view image taken after the milling had been completed.

The device 300–1 on Wafer S-2, whose location was overlapping with the features observed in XRT image (device marked by rectangular box in Fig. 4b), was similarly progressively milled in cross section across an area of 40 µm × 30 µm. This particular device had suffered premature breakdown and showed crater-like surface damage, as marked by the arrow in Fig. 11a. This crater-like pit was 100 µm long, almost 50 µm wide at its center, and

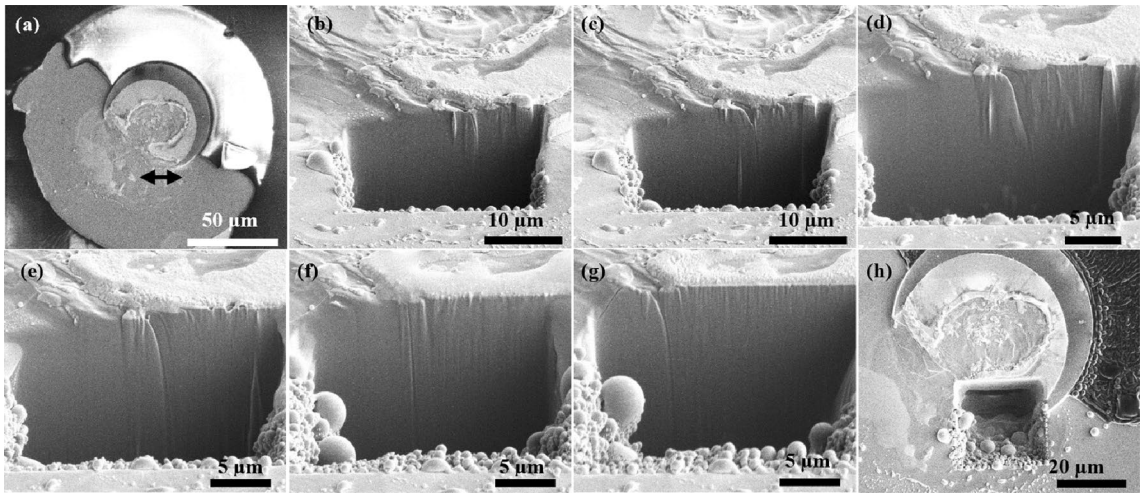

Fig. 10 Series of SEM images of device 60–2 on Wafer S-3, showing progressive cross-sectional milling across a surface area of 25 µm (length) × 25 µm (depth): (a) plan-view image also showing the location where milling started (double-arrow line); (b–g) cross-sectional images each taken after milling away another 5 µm, clearly showing the presence of dislocations extending deep into the substrate; (h) plan-view image taken after completion of milling.

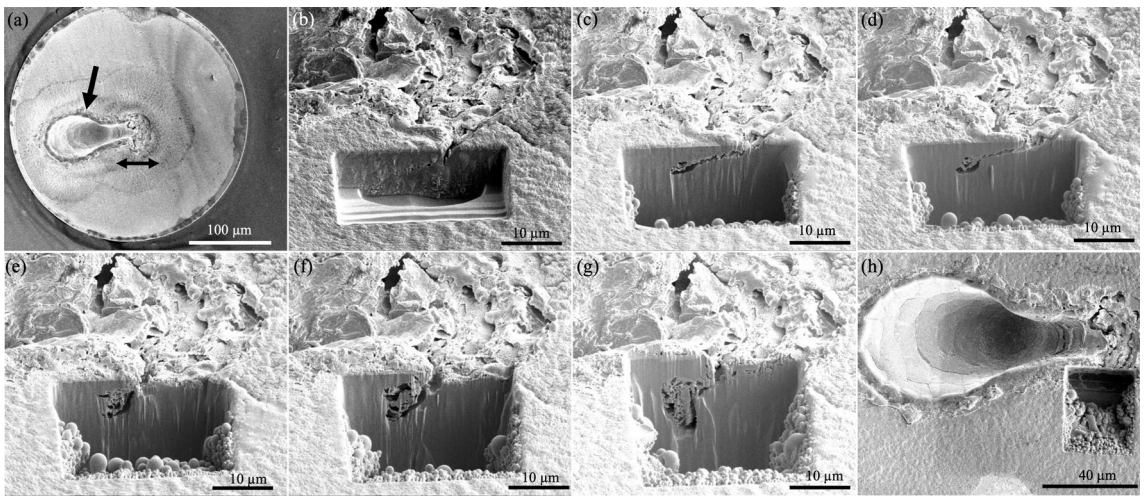

Fig. 11 Series of SEM images of device 300–1 on Wafer S-2, showing progressive cross-sectional milling across surface area of 40 µm (length) × 30 µm (depth): (a) plan-view image showing the location where milling started (double-arrow line) and a crater-like surface pit (arrow); (b–g) cross-sectional images each taken after 5 µm of milling, showing the presence of a cluster of voids and dislocations; (h) plan-view image taken after completion of milling.

almost 30 µm deep. The series of SEM images shown in Fig. 11b–g reveal the presence of threading dislocations penetrating deep into the substrate as well as clusters of voids, similar to results reported elsewhere.[34] Similar progressive milling that was undertaken on diodes with high reverse-bias voltages (> 300 V) showed an absence of dislocations or voids. These results are in agreement with previous studies where diodes that had been reverse-bias stressed to failure showed the presence of dislocations, cracks, and voids in SEM and TEM images.[34]

Summary and Conclusions

This paper has described the effects of substrate morphology on the reverse-bias electrical behavior of fabricated GaN *p-i-n* diode devices. Two HVPE substrates, which originated from two different sources, revealed near-surface features when observed by XRT. Fabricated devices that overlapped with these features had low reverse-bias voltages, whereas devices located away from such features

had comparatively much higher reverse-bias voltages for a leakage current limit set at 10^{-6} A. In comparison, an ammonothermal substrate showed no surface features when observed by XRT. However, not all diodes fabricated on this substrate had similar performance. The HVPE-grown Wafer S-1 showed a two-dimensional array of equally spaced dark spots, and devices that overlapped with these features had low threshold cutoff voltages, whereas devices located elsewhere had voltages that exceeded 300 V at the set current limit. The HVPE-grown Wafer S-2 showed equally spaced vertical and discontinuous surface features. Similar to Wafer S-1, diodes overlapping with these features had low threshold voltages, and diodes located away had high voltages (> 300 V). Even though ammonothermal-grown Wafer S-3 showed no such surface features, some diodes fabricated on this wafer had low voltages (50–200 V), while some diodes had high voltages (> 320 V). Surface etching on a wafer similar to S-1 showed clusters of hexagonal-shaped pyramidal pits. Diodes with premature breakdown fabricated on ammonothermal-grown Wafer S-3 and HVPE-grown Wafer S-2 showed visible irreversible surface damage. Some of these failed devices showed deep crater-like damage which was ~ 30 microns deep. Progressive ion milling on these devices revealed the presence of threading dislocations extending further into the substrate (~ 26 microns) and clusters of voids. Similar progressive ion milling on devices with high voltages showed no dislocations or voids. Overall, this work provides valuable information on the relationship between the breakdown voltage and the morphology of GaN substrates, which can serve as an important reference for developing high-voltage and reliable GaN-on-GaN vertical devices for GaN power electronics.

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Conflict of interest The authors declare that they have no conflict of interest.

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