GaN-Based Threshold Switching Behaviors at High Temperatures Enabled by Interface Engineering for Harsh Environment Memory Applications

Kai Fu, Shisong Luo, Houqiang Fu, *Member, IEEE*, Kevin Hatch, Shanthan Reddy Alugubelli, Hanxiao Liu, Tao Li, Mingfei Xu, Zhaobo Mei, Ziyi He, Jingan Zhou, Cheng Chang, Fernando A. Ponce, Robert Nemanich, and Yuji Zhao, *Member, IEEE*

***Abstract*— We demonstrate threshold switching behaviors with working temperatures up to 500 °C based on GaN vertical p-n diodes, and these devices survived a passive test in a simulated Venus environment (460 °C, 94 bar, CO_2 gas flow) for ten days. This is realized via interface engineering through an etch-then-regrow process combination with a Ga_2O_3 interlayer. It is hypothesized the traps in the interfacial layer can form/rupture a conductive path by trapping/detrapping electrons/holes, which are responsible for the observed threshold switching behaviors. To the best of our knowledge, this is the first demonstration of two-terminal threshold-switching memory devices under such high temperatures. These results can serve as a critical reference for the future development of GaN-based memory devices for harsh environment applications.**

***Index Terms*— Ga_2O_3, GaN, harsh environment, high temperature, interface engineering, memory, p-n diodes, threshold switching, Venus, wide bandgap semiconductor.**

Manuscript received 16 September 2023; accepted 29 September 2023. Date of publication 10 October 2023; date of current version 1 March 2024. This work was supported in part by NASA HOTTech Program under Grant 80NSSC17K0768; in part by ULTRA, an Energy Frontier Research Center through the U.S. Department of Energy (DOE), Office of Science, Basic Energy Sciences (BES), under Award DE-SC0021230; in part by CHIMES, one of the Seven Centers in JUMP 2.0, a Semiconductor Research Corporation (SRC) Program by DARPA; in part by the NanoFab through NSF under Contract ECCS-1542160; and in part by the National Science Foundation (NSF) under Award 2302696. The review of this article was arranged by Editor F. Medjdoub. *(Kai Fu and Shisong Luo contributed equally to this work.) (Corresponding authors: Kai Fu; Yuji Zhao.)*

Kai Fu is with the School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ 85287 USA, also with the Department of Electrical and Computer Engineering, Rice University, Houston, TX 77005 USA, and also with the Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112 USA (e-mail: kai.fu@utah.edu).

Shisong Luo, Tao Li, Mingfei Xu, Zhaobo Mei, and Cheng Chang are with the Department of Electrical and Computer Engineering, Rice University, Houston, TX 77005 USA.

Houqiang Fu and Ziyi He are with the School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ 85287 USA.

Kevin Hatch, Shanthan Reddy Alugubelli, Hanxiao Liu, Fernando A. Ponce, and Robert Nemanich are with the Department of Physics, Arizona State University, Tempe, AZ 85287 USA.

Jingan Zhou and Yuji Zhao are with the School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ 85287 USA, and also with the Department of Electrical and Computer Engineering, Rice University, Houston, TX 77005 USA (e-mail: yuji.zhao@rice.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3321562.

Digital Object Identifier 10.1109/TED.2023.3321562

I. Introduction

RECENT years have seen intensive research interests in resistive random access memory (RRAM) from both industries and academia due to its great potential in non-volatile memory (NVM) [1], neuromorphic computing [2], [3], compute-in-memory systems [4], and artificial intelligence [5]. RRAM has excellent scalability, fast write/read speed, and low programming voltage, which is beneficial for large-scale and high-density NVM. There are two major RRAM array structures: one transistor and one resistor (1T1R) and crossbar. Compared with the 1T1R arrays, crossbar arrays, consisting of rows and columns perpendicular to each other with RRAM cells sandwiched in between, exhibit smaller cell area and better scalability, but the sneak path current through unselected cells in the array presents a significant challenge due to the degradation of read and write margin and increased power consumption. To reduce the sneak path, the threshold switching selectors with strong I–V nonlinearities are desired to be added in series with RRAM cell [6], [7], [8], [9].

Many oxides have exhibited resistive and threshold switching behaviors [10], [11], [12], such as TiO_x, ZnO_x, NiO, AlO_x, TiN/HfO_2, and so on. However, most of the reported devices showed a working temperature of below 200 °C and radiation sensitivity, which limit their potential applications in harsh environments, such as space and high temperatures [13]. Recently, III-nitrides have also been reported to show resistive switching behaviors [14], [15]. III-nitride materials are thermally and chemically stable and have already been widely used in various optoelectronics and electronics, e.g., light-emitting diodes [16], [17], power electronics [18], [19], and high-temperature mixed-signal and RF electronics

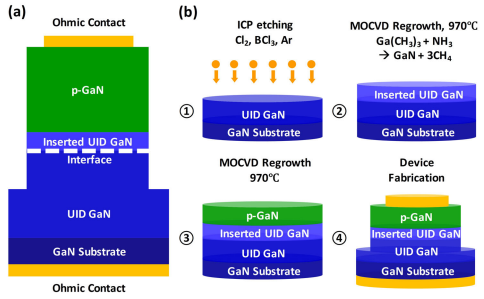

Fig. 1. (a) Schematic cross section of the GaN diode. (b) Schematics of the fabrication process of GaN diode based on etch-then-regrow process.

[20], [21], [22], [23]. Developing high-performance III-nitride-based threshold switching devices can open doors for new generation GaN-based RRAM arrays and integrated circuits in harsh environments.

In this work, we demonstrate the GaN-based threshold switching behaviors with stable high-temperature performance up to 500 °C for the first time, which is much higher than our previous report [24]. They also survived a passive test in a simulated Venus environment for ten days.

II. GaN Threshold Switching Behaviors

As shown in Fig. 1, the GaN p-n diodes were fabricated by an etch-then-regrow process. Samples were homoepitaxially grown by MOCVD on c-plane n-GaN substrates. An unintentionally doped (UID) GaN (4 μm, 10^{16} cm^{-3}) was first grown on the GaN substrate. Then, 500-nm GaN was etched away to form an etched surface by ICP, followed by 50-nm UID-GaN as an insertion layer and 1-μm p-GaN successively regrown on the etched surface by MOCVD. The top and bottom electrodes were formed by metal stacks of Pd/Ni/Au and Ti/Al/Ni/Au, respectively. The etch-then-regrow process introduced a large amount of Si and O atoms according to secondary-ion-mass spectrometry results and an interfacial layer was formed after the etch-then-regrow process according to transmission electron microscopy results, which has been reported in our previous works [25], [26].

Fig. 2(a) shows the resistive switching characteristics of the GaN diode after the forming process through a soft reverse breakdown. The threshold voltage (V_{th}) was 14 V and hold voltage (V_{hold}) was 4 V, which were universally observed for multiple devices. We could also calculate the ON current density of 40 A/cm^2 and OFF current density of 0.4 A/cm^2 after dividing the current by the device's area. The threshold switching behavior was only observed at positive bias since the device contains a p-n diode. Due to this fact, the emission of blue light from the p-n junction could also be used as an indicator for the switching process between the ON state and the OFF state [Fig. 2(b)]. This device could robustly work at 25 °C–300 °C and survive 1000 cycles test at 300 °C, which has been reported in our previous work [24].

The current at V_{th} at the OFF state as a function of temperature is shown in Fig. 2(c). The decrease in the current with increasing temperatures is due to a thermal detrapping effect.

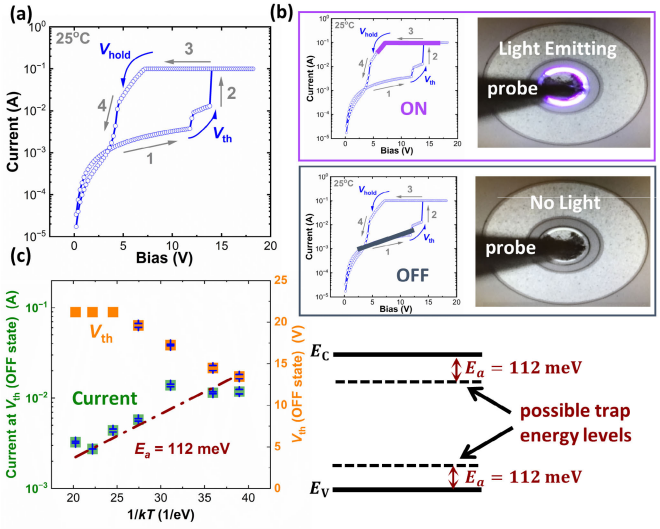

Fig. 2. (a) I–V curve of GaN diode after the forming process. Numbers and arrows indicate the sequence of voltage sweeping. (b) Top: ON state of GaN selector with light emission. Bottom: OFF state without light emission. (c) Current at V_{th} as a function of temperature. The thermal activation energy for the detrapping process is 112 meV.

The temperature dependence of the current can be expressed as follows [27]:

$$I = I_0 \exp\left(\frac{E_a}{kT}\right) \tag{1}$$

where k is the Boltzmann constant and E_a is the thermal activation energy. E_a refers to the thermal detrapping energy in this work, which is 112 meV by fitting the experimental data. In our previous study, we reported that trap-assisted space charge limited current theory could explain the I–V characteristic in Fig. 2(a) [24]. Furthermore, as shown in Fig. 2(c), the energy difference between detrapping energy level and E_C/E_V is 112 meV.

Expired by trap-assisted space charge limited current theory, we proposed a physical mechanism to explain the observed threshold switching behaviors in the GaN diode [28], [29]. Electron/hole traps in the interfacial layer form/rupture a conductive path by trapping/detrapping electrons/holes. Energy band diagrams for the GaN diode at different voltages are shown in Fig. 3. Before the forming process, the device behaves like a conventional p-n diode [Fig. 3(a)]. The details of the forming process have been reported in our previous work [24]. After the forming process, an insulation layer containing many traps may form at the regrowth interface [Fig. 3(b)]. When a low positive bias ($<V_{\text{hold}}$) is applied to the device, the positive bias mainly drops across the p-n junction and then the insulation layer [Fig. 3(c)]. Therefore, the current of the device is very low and the device is at OFF state. Meanwhile, the electrons/holes are trapped by the interfacial traps [Fig. 3(d)], and therefore, the emission of blue light is not observed. When the positive bias increases to V_{th}, a conductive path forms by trapping enough electrons/holes [Fig. 3(e)]. Then, the insulator behaves like a conductive layer with low resistance and the device behaves like a conventional p-n diode (ON state). The emission of blue light is observed

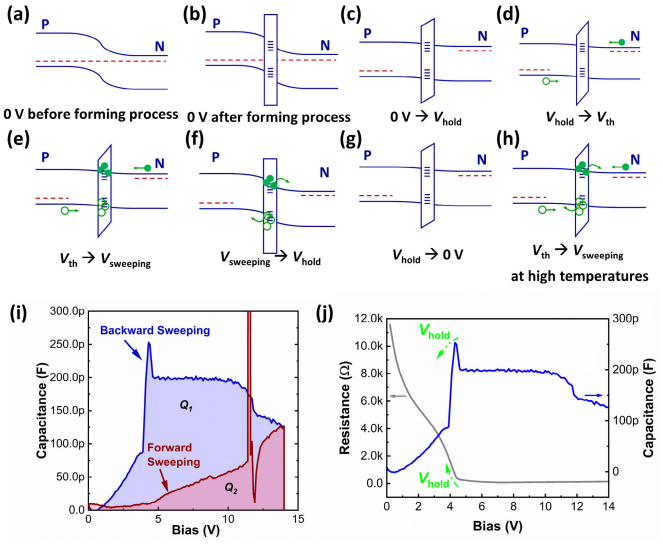

Fig. 3. Energy band diagrams for GaN diode at different voltages. (a) No insulation layer before the forming process. (b) Insulation layer forms at the regrowth interface after the forming process. (c) Voltage drops on the p-n junction and insulation layer. (d) Injection happens. (e) Conductive path forms due to the injection when above V_{th}. (f) Device behaves like a traditional p-n diode and detrapping happens. (g) Conductive path disappears due to the detrapping. (h) High temperature enhances the detrapping. (i) C–V characteristics of forward and backward sweeping. (j) Resistance and capacitance of backward sweeping.

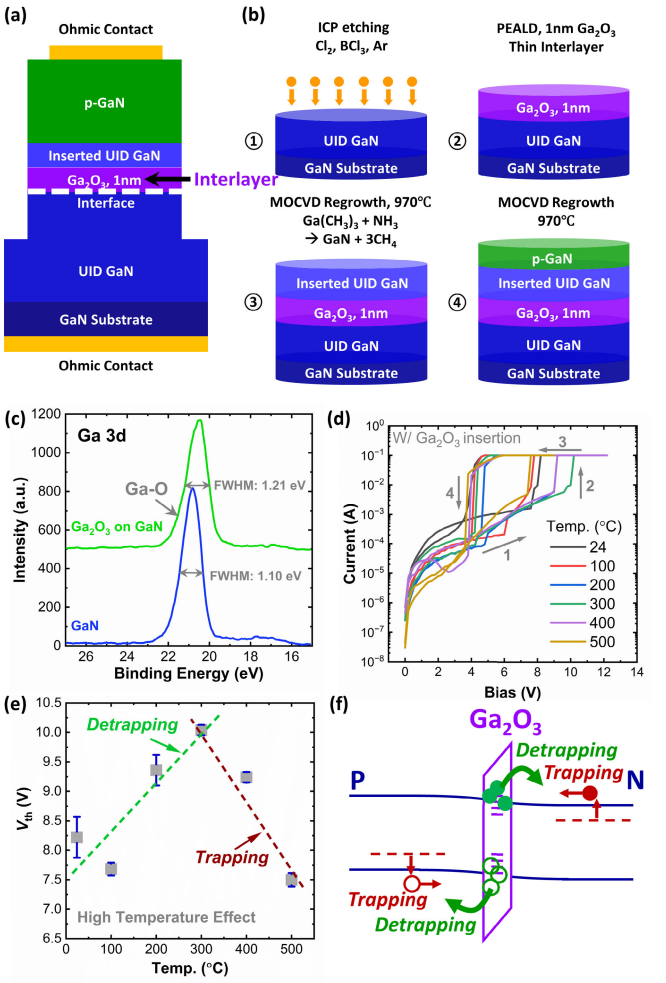

Fig. 4. (a) Schematic cross section of the GaN diode with a Ga_2O_3 interlayer. (b) Schematics of the fabrication process of GaN diode with a Ga_2O_3 interlayer. (c) XPS spectra of Ga 3d for the sample surface before and after depositing 1-nm Ga_2O_3. (d) I–V curves of GaN selectors with a Ga_2O_3 interlayer at 24 °C–500 °C. (e) V_{th} as a function of temperature for the GaN diode with a Ga_2O_3 interlayer. (f) Energy band diagram of GaN diode with a Ga_2O_3 interlayer.

until the voltage decreases to V_{hold} [Figs. 2(b) and 3(f)]. When the voltage continues to decrease below V_{hold}, few carriers are trapped by the traps because the p-n junction is turned off, i.e., OFF state [Fig. 3(g)]. With increasing temperature, more electrons/holes detrap from interfacial traps to the conduction/valence band and then drift to n-GaN/p-GaN under the built-in electrical field in the diode's space charge region. The direction of the drift current origin from detrapping is opposite to that of the injection current [Fig. 3(h)]. Therefore, V_{th} increases and I_{off} decreases with increasing temperature. The decrease of current at the OFF state with increasing temperature is also due to the thermal detrapping effect. Besides, because most of the voltages drop on the p-n diode at the reverse bias, the threshold switching behavior is negligible at the reverse bias.

The C–V characteristics of forward and backward sweeping are conducted to support the above mechanics. Fig. 3(i) shows a clear difference in integral areas of capacitance–voltage (C–V) curves by forward and backward sweeping. This indicates that a lot of charges were trapped during voltage sweeping from OFF state to ON state. Specifically, the trapped charges (Q_1) are approximately 1.26 nC. According to the forward sweeping C–V curve, the injection charge (Q_2) is 0.72 nC when bias increases from 0 to 14 V. When the bias is higher than 14 V, the conductive path will form, and this is the reason why a V_{th} of 14 V is obtained in Fig. 2(a). According to the backward sweeping I–V curve in Fig. 2(a) and C–V curve in Fig. 3(i), the device's resistance and capacitance during backward sweeping are illustrated in Fig. 3(j). A sharp increase in resistance and a decrease in capacitance are observed from 4.5 to 3.5 V, indicating the conductive path disappearance. This is the origin of V_{hold} at 4 V. Therefore, our proposed physical mechanism could explain these experimental phenomena.

III. Enhanced High-Temperature Performance

The device based on the etch-then-regrow process can work up to 300 °C. However, the threshold switching behavior disappeared at higher than 350 °C due to the strong thermal detrapping effect. Meanwhile, based on the mechanism discussed above, the key factor for the GaN threshold switching behavior is the interfacial layer with traps. Therefore, an intentional interlayer could be helpful to make the device more controllable with better high-temperature performance.

As the native oxide of GaN, Ga_2O_3 is a promising candidate for the interfacial layer with a small lattice mismatch (<5%). Fig. 4(a) and (b) shows the fabrication process of diodes with 1-nm Ga_2O_3 as the interlayer by plasma-enhanced atomic layer deposition (PEALD). Trimethylgallium (TMG) and O_2 plasma were used to grow Ga_2O_3 at 200 °C. TMG (99.998%, Strem

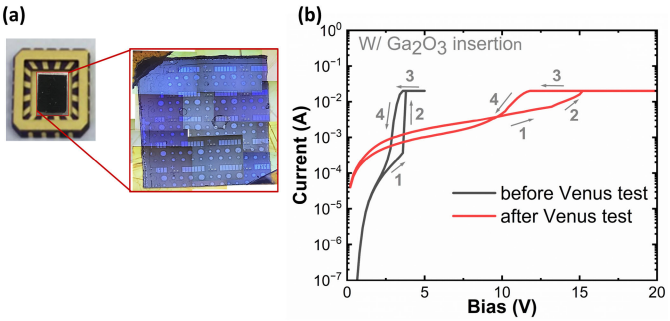

Fig. 5. (a) DUT placed in simulated Venus's environment for the passive test. (b) *I*–*V* curve before and after the passive test.

Chemicals, Inc.) was used as the Ga source and delivered into the reactor using Ar carrier gas (99.999%) with a flow rate 2.0 sccm, resulting in a pressure transient of 200 mtorr. TMG was pulsed for 0.1 s into Ar carrier gas, followed by a 30-s exposure. The chamber was purged between exposures for 30 s using a 30.0-sccm N_2 (99.999%) flow. O_2 plasma was generated using a 13.56-MHz RF generator with an O_2 (99.999%) flow rate of 30.0 sccm. A throttling valve is used to maintain a pressure of 100 mtorr. O_2 pressure stabilized for 5 s before plasma ignition, followed by 100-W plasma exposure for 10 s. Further description of this PEALD process has been reported [30]. The broadening of the Ga 3d peak in XPS spectra shows the bonding of Ga to O [Fig. 4(c)]. The Ga_2O_3 interlayer was found to be effective in improving the high-temperature performance of the selector, which can work up to 500 °C [Fig. 4(d)]. The decrease of V_{th} could be explained by the reduced trapped charges after introducing Ga_2O_3. V_{th} of the device first increased and then decreased with increasing temperatures [Fig. 4(e)]. This nonlinear variation is due to the thermally enhanced detrapping and trapping processes [Fig. 4(f)]. According to the explanation of Fig. 3(h), the detrapping from interfacial traps increased V_{th} at 25 °C–300 °C. At 300 °C–500 °C, thermally activated intrinsic carrier densities in p GaN and n GaN increased rapidly. The injection of thermal activation carriers into traps decreased the V_{th}.

The device under test (DUT) was placed in a simulated Venus environment (460 °C, 94 bar, CO_2 gas flow) over ten days in the University of Arkansas chamber [Fig. 5(a)]. A comparison of the *I*–*V* curves reveals that the threshold switching behavior of the device was maintained even though there is without passivation, which indicates that this device is a promising candidate for selector in NVM or volatile memory for harsh environment applications. However, V_{th} and V_{hold} are significantly increased [Fig. 5(b)], which might be caused by p-GaN conductivity degradation, surface damage, increased trapping density at the regrown interface, and/or electrode metal degradation after a harsh environment test, and the performance should be more stable. Introducing suitable passivation layer could improve the stability by maintaining the p-GaN conductivity and protecting the device surface from thermal damage and consequently improve the device's robustness operation in harsh environments. It should be noted that the trapped charges varied at devices. Therefore, V_{th} of the device in Fig. 5(b) is different from that in Fig. 4(d).

TABLE I
SUMMARY OF GAN-BASED HIGH-TEMPERATURE MEMORY

Ref	Two terminal or multi terminal memory	Memory cell	Highest Temp (°C)	Active or passive test in simulated Venus environment
[30] 2021	Multi terminal	6 transistor SRAM	300	-
[31] 2021		D flip-flop	160	-
[32] 2022		1 transistor	200	-
[21] 2023		D flip-flop	500	-
[24] 2019		p-n diode	300	-
This work	**Two terminal**	**p-n diode with Ga_2O_3 interlayer**	**500**	**Passive test**

A summary of GaN-based high-temperature memory reported in the literature is presented in Table I. To the best of our knowledge, this is the first demonstration of two-terminal GaN-based memory with working temperatures up to 500 °C and surviving a passive test in a simulated Venus environment.

IV. CONCLUSION

GaN-based threshold switching selectors working up to 500 °C were realized via interface engineering through an etch-then-regrow process in combination with a Ga_2O_3 interlayer. It is hypothesized that the traps in the interfacial layer can form/rupture a conductive path by trapping/detrapping electrons/holes, which are responsible for the observed threshold switching behavior. The addition of Ga_2O_3 interlayer prior to the regrowth can remarkably improve the selector thermal performance. The device threshold switching behavior was maintained after a passive test in a simulated Venus environment chamber over ten days. The result is an important reference for developing GaN-based memory devices for harsh environment applications.

ACKNOWLEDGMENT

The authors would like to thank the use of facilities within the Eyring Materials Center at Arizona State University and the chamber with a simulated Venus environment at the University of Arkansas. The device fabrication was performed at the Eyring Materials Center at Arizona State University.

REFERENCES

[1] H.-S. P. Wong et al., "Metal–oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012, doi: 10.1109/JPROC.2012.2190369.
[2] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, and H.-S.-P. Wong, "A neuromorphic visual system using RRAM synaptic devices with sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling," in *IEDM Tech. Dig.*, Dec. 2012, p. 10, doi: 10.1109/IEDM.2012.6479018.
[3] S. Yu, P.-Y. Chen, Y. Cao, L. Xia, Y. Wang, and H. Wu, "Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect," in *IEDM Tech. Dig.*, Dec. 2015, p. 17, doi: 10.1109/IEDM.2015.7409718.
[4] W. Wan et al., "A compute-in-memory chip based on resistive random-access memory," *Nature*, vol. 608, no. 7923, pp. 504–512, Aug. 2022, doi: 10.1038/s41586-022-04992-8.

[5] S. Thomas, "Artificial intelligence on a resistive RAM chip," *Nature Electron.*, vol. 5, no. 9, p. 544, Sep. 2022, doi: 10.1038/s41928-022-00846-3.

[6] S. Yu, *Resistive Random Access Memory (RRAM): From Devices to Array Architectures* (Synthesis Lectures on Emerging Engineering Technologies), vol. 2, no. 5. Cham, Switzerland: Springer, Mar. 2016, pp. 1–79, doi: 10.1007/978-3-031-02030-8.

[7] J. Yoo, J. Woo, J. Song, and H. Hwang, "Threshold switching behavior of Ag-Si based selector device and hydrogen doping effect on its characteristics," *AIP Adv.*, vol. 5, no. 12, Dec. 2015, Art. no. 127221, doi: 10.1063/1.4938548.

[8] K. Lee et al., "Flexible resistive random access memory devices by using NiO_x/GaN microdisk arrays fabricated on graphene films," *Nanotechnology*, vol. 28, no. 20, May 2017, Art. no. 205202, doi: 10.1088/1361-6528/aa6763.

[9] J. Song, J. Woo, A. Prakash, D. Lee, and H. Hwang, "Threshold selector with high selectivity and steep slope for cross-point memory array," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 681–683, Jul. 2015, doi: 10.1109/LED.2015.2430332.

[10] S. Lim, J. Yoo, J. Song, J. Woo, J. Park, and H. Hwang, "Excellent threshold switching device (I_{off} ~ 1 pA) with atom-scale metal filament for steep slope (<5 mV/dec), ultra low voltage (V_{dd} = 0.25 V) FET applications," in *IEDM Tech. Dig.*, Dec. 2016, p. 34, doi: 10.1109/IEDM.2016.7838543.

[11] D.-H. Kwon et al., "Atomic structure of conducting nanofilaments in TiO_2 resistive switching memory," *Nature Nanotechnol.*, vol. 5, no. 2, pp. 148–153, Feb. 2010, doi: 10.1038/nnano.2009.456.

[12] P. Calka et al., "Chemical and structural properties of conducting nanofilaments in TiN/HfO_2-based resistive switching structures," *Nanotechnology*, vol. 24, no. 8, Feb. 2013, Art. no. 085706, doi: 10.1088/0957-4484/24/8/085706.

[13] M. Wang et al., "Robust memristors based on layered two-dimensional materials," *Nature Electron.*, vol. 1, no. 2, pp. 130–136, Feb. 2018, doi: 10.1038/s41928-018-0021-4.

[14] Y. Liu, T. P. Chen, P. Zhao, S. Zhang, S. Fung, and Y. Q. Fu, "Memory effect of Al-rich AlN films synthesized with RF magnetron sputtering," *Appl. Phys. Lett.*, vol. 87, no. 3, Jul. 2005, Art. no. 033112, doi: 10.1063/1.2000337.

[15] Y. Chen et al., "Reproducible bipolar resistive switching in entire nitride AlN/n-GaN metal-insulator-semiconductor device and its mechanism," *Appl. Phys. Lett.*, vol. 105, no. 19, p. 19350, Nov. 2014, doi: 10.1063/1.4901747.

[16] J. Xue et al., "Thermally enhanced blue light-emitting diode," *Appl. Phys. Lett.*, vol. 107, no. 12, Sep. 2015, Art. no. 121109, doi: 10.1063/1.4931365.

[17] Y. Zhao et al., "High-power blue-violet semipolar (2021) InGaN/GaN light-emitting diodes with low efficiency droop at 200 A/cm^2," *Appl. Phys. Exp.*, vol. 4, no. 8, Jul. 2011, Art. no. 082104, doi: 10.1143/apex.4.082104.

[18] H. Fu, K. Fu, S. Chowdhury, T. Palacios, and Y. Zhao, "Vertical GaN power devices: Device principles and fabrication technologies—Part II," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3212–3222, Jul. 2021, doi: 10.1109/TED.2021.3083209.

[19] K. Fu, Z. He, C. Yang, J. Zhou, H. Fu, and Y. Zhao, "GaN-on-GaN p-i-n diodes with avalanche capability enabled by eliminating surface leakage with hydrogen plasma treatment," *Appl. Phys. Lett.*, vol. 121, no. 9, Aug. 2022, Art. no. 092103, doi: 10.1063/5.0107677.

[20] M. Yuan et al., "GaN ring oscillators operational at 500 °C based on a GaN-on-Si platform," *IEEE Electron Device Lett.*, vol. 43, no. 11, pp. 1842–1845, Nov. 2022, doi: 10.1109/LED.2022.3204566.

[21] Q. Xie et al., "Towards DTCO in high temperature GaN-on-Si technology: Arithmetic logic unit at 300 °C and CAD framework up to 500 °C," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2023, pp. 1–2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185364.

[22] D. Maier et al., "InAlN/GaN HEMTs for operation in the 1000 °C regime: A first experiment," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 985–987, Jul. 2012, doi: 10.1109/LED.2012.2196972.

[23] M. Yuan et al., "Enhancement-mode GaN transistor technology for harsh environment operation," *IEEE Electron Device Lett.*, vol. 44, no. 7, pp. 1068–1071, Jul. 2023, doi: 10.1109/LED.2023.3279813.

[24] K. Fu et al., "Threshold switching and memory behaviors of epitaxially regrown GaN-on-GaN vertical p-n diodes with high temperature stability," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 375–378, Mar. 2019, doi: 10.1109/LED.2019.2891391.

[25] K. Fu et al., "Investigation of GaN-on-GaN vertical p-n diode with regrown p-GaN by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 113, no. 23, Dec. 2018, Art. no. 233502, doi: 10.1063/1.5052479.

[26] K. Fu et al., "Demonstration of 1.27 kV etch-then-regrow GaN p-n junctions with low leakage for GaN power electronics," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1728–1731, Nov. 2019, doi: 10.1109/LED.2019.2941830.

[27] Y. C. Yang, F. Pan, Q. Liu, M. Liu, and F. Zeng, "Fully room-temperature-fabricated nonvolatile resistive memory for ultrafast and high-density memory application," *Nano Lett.*, vol. 9, no. 4, pp. 1636–1643, Apr. 2009, doi: 10.1021/nl900006g.

[28] F.-C. Chiu, "A review on conduction mechanisms in dielectric films," *Adv. Mater. Sci. Eng.*, vol. 2014, pp. 1–18, Feb. 2014, doi: 10.1155/2014/578168.

[29] M. A. Lampert, "Simplified theory of space-charge-limited currents in an insulator with traps," *Phys. Rev.*, vol. 103, no. 6, pp. 1648–1656, Sep. 1956, doi: 10.1103/PhysRev.103.1648.

[30] N. Chowdhury, J. Jung, Q. Xie, M. Yuan, K. Cheng, and T. Palacios, "Performance estimation of GaN CMOS technology," in *Proc. Device Res. Conf. (DRC)*, Jun. 2021, pp. 1–2, doi: 10.1109/DRC52342.2021.9467201.

[31] A. Hassan, J.-P. Noël, Y. Savaria, and M. Sawan, "Circuit techniques in GaN technology for high-temperature environments," *Electron.*, vol. 11, no. 42, pp. 1–22, Dec. 2021, doi: 10.3390/electronics11010042.

[32] T. Chen, Z. Zheng, S. Feng, L. Zhang, W. Song, and K. J. Chen, "GaN non-volatile memory based on junction barrier-controlled bipolar charge trapping," *IEEE Electron Device Lett.*, vol. 43, no. 5, pp. 697–700, May 2022, doi: 10.1109/LED.2022.3161010.